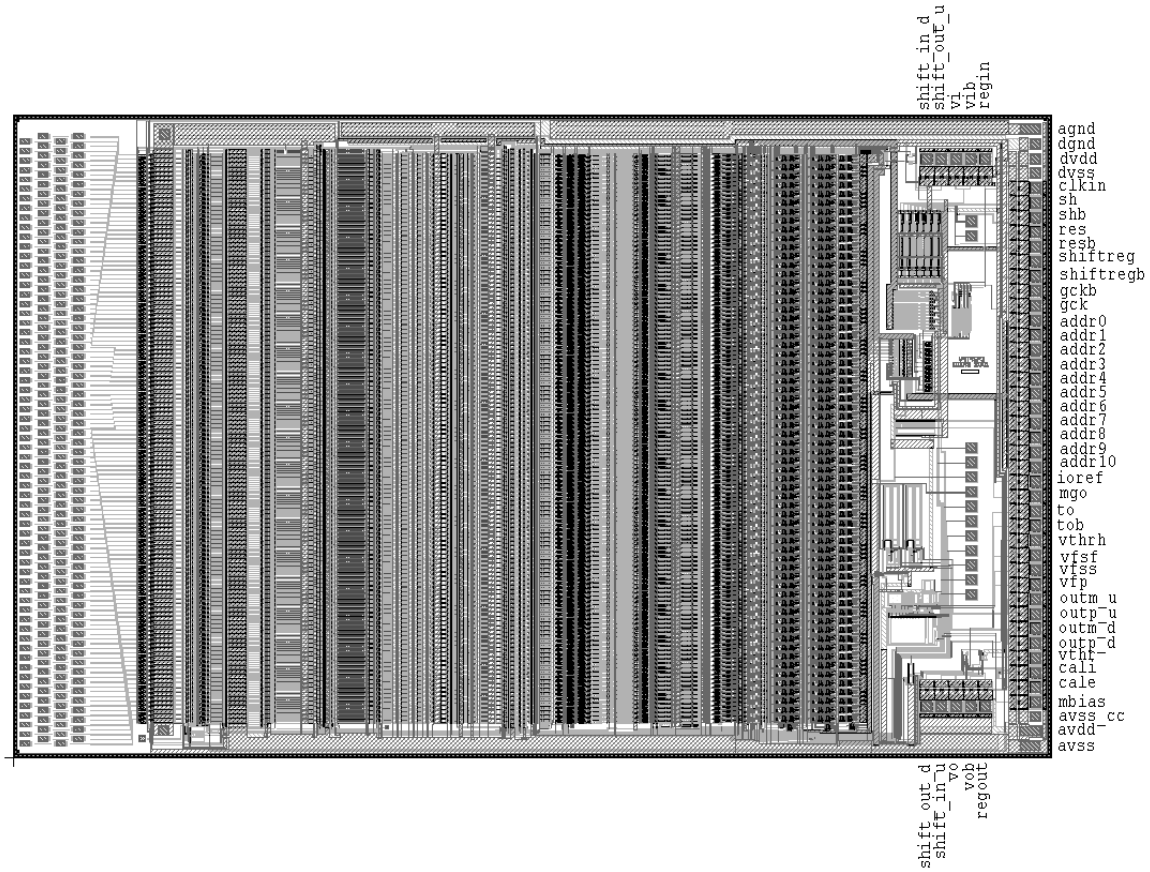
VaTagp3

Specifications (preliminary) V0.91



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1 General

The VaTaGP3 is a 128-channel “general purpose” charge sensitive amplifier. Each channel features low-noise/low-power buffered preamplifiers, a shaper with sample/hold, multiplexed analogue readout and calibration facilities. In addition, each channel has a fast shaper that gives a trigger signal. The analogue value and the address of the trigging channels are read out with a flexible serial or sparse read-out system. The VaTaGP3 also offers input leakage current compensation automatically adjusted in each preamplifier channel.

The VaTaGP3 is designed for use in systems employing many chips in parallel, sharing some control lines and all output lines with the other modules.

2 Physical

Process:	0.8 µm N-well CMOS, double poly, double metal.	
Die size:	9895 µm x 6120 µm (including scribe) Thickness: ~ 600 µm	
Input bonding pads:	Double row.	
	Pad size:	90 µm x 50 µm
	Pad pitch:	91.2 µm (see Figure 3)
	Pad pitch, net:	45.6 µm (see Figure 3)
Control, output, biasing and power pads:	Single row.	
	Pad size:	90 µm x 90 µm
	Pad pitch:	140 µm (see Figure 2)

3 Electrical

Simulated values, to be verified by measurements.

Power rails:	Vdd = +2 V, Vss = -2 V, Gnd = 0 V. Each with separate connections for analogue (avdd, avss and agnd) and digital sections (dvdd, dvss and dgnd) of the chip.	
Back contact:	Connect to avss (-2V)	
Current description: (Quiescent, typical values with mbias=500 uA)	dvdd dvss dgnd avdd avss agnd	~3 mA? ~6 mA? 0 mA ~50 mA? ~100 mA? ~50 mA?
Input bias currents:	Nominal values	
mbias	500 uA	all other biases are internally generated and can be unconnected
Power dissipation: (Typical values)	Quiescent:	300 mW (2.3 mW/channel)??

Gain:	~44µA/fC (differential branches added).
DNR:	~±18fC
Peaking time, slow shaper	3 us
Peaking time, fast shaper	~150 ns

4 Pad Description

Bias pads which do not require bonding (internally generated or pull-up/pull-down) can be bonded for external decoupling, adjustment or forcing. Pads described clock-wise from upper left to lower left (excluding input pads). Positive current direction into the chip.

Pad-row on the ASIC top side:

Pad name	Type	Description	Nominal value
shift_in_d	di	Shiftregister input (downwards)	logical
shift_out_u	do	Shiftregister output (upwards)	logical
vi	ldi	Veto input (pos. phase)	low v. logical (pd)
vib	ldi	Veto input (neg. phase)	low v. logical (pu)
regin	di	Data input for control register	logical (pd)

Pad-row on the ASIC right side:

Pad name	Type	Description	Nominal value
AGND	p	Signal ground for the analogue part	0 V
DGND	p	Connect to AGND	0 V
DVDD	p	Digital vdd	2 V
DVSS	p	Digital vss	-2 V
clkin	di	Clock for control register	logical
sh	ldi	Sample and hold (pos. phase)	low v. logical
shb	ldi	Sample and hold (neg. phase)	low v. logical
res	ldi	Reset of the readout logic (pos. phase)	low v. logical (pd)
resb	ldi	Reset of the readout logic (neg. phase)	low v. logical (pu)
shiftreg	ldi	Readout mode (pos. phase)	low v. logical (pu)
shiftregb	ldi	Readout mode (neg. phase)	low v. logical (pd)
gckb	ldi	Clock for readout (neg. phase)	low v. logical
gck	ldi	Clock for readout (pos. phase)	low v. logical
addr0-6	do	Digital output of hit channel address	Current (100 uA)
:	:	:	:
addr7-10	do	Digital output of chip address	Current (100 uA)
ioref	ai	Current sink for the address output buffer	Connect to ~0V
mgo	ao	Multi-hit trigger output	current
to	do	Trigger out (positive phase)	current
tob	do	Trigger out (negative phase)	current
vthrh	ai	High threshold for the discriminator	2V /-2V? (depending on signal polarity)
vfsf	ai	Control voltage for the feedback resistor (NMOS) in the fast shaper	200 mV (int. gen.)

vfss	ai	Control voltage for the feedback resistor (NMOS) in the slow shaper	150 mV (int. gen.)
vfp	ai	Control voltage for the feedback resistor (NMOS) in the preamplifier	-300 mV (int. gen.)
outm_u	ao	Diff. analog output, neg. phase (upwards shiftregister)	0-200 uA
outp_u	ao	Diff. analog output, pos. phase (upwards shiftregister)	0-200 uA
outm_d	ao	Diff. analog output, neg. phase (downwards shiftregister)	0-200 uA
outp_d	ao	Diff. analog output, pos. phase (downwards shiftregister)	0-200 uA
vthr	ai	Normal threshold for the discriminator	⇑ 50 mV?
cali	ai	Test pulse with internal capacitor	voltage step
cale	ai	Test pulse with external capacitor	charge
mbias	ai	Bias reference for all the internally generated biases	500 uA
AVSS_CC	ai	Reference for current compensation	–2V
AVDD	p	Analog vdd	2 V
AVSS	p	Analog vss	-2 V

Pad-row on the ASIC bottom side:

Pad name	**Type**	**Description**	**Nominal value**
regout	do	Data output of the control register	logical
vob	ldo	Veto output (neg. phase)	low v. logical
vo	ldo	Veto output (pos. phase)	low v. logical
shift_in_u	di	Shiftregister input (upwards)	logical
shift_out_d	do	Shiftregister output (downwards)	logical

Inner control pad row, from upper to lower:

Pad name	**Type**	**Description**	**Nominal value**
Dlt	ldi	Inhibit further trigger generation, pos.phase.	Internally pulled low
Dltb	ldi	Inhibit further trigger generation, neg. phase.	Internally pulled high

p = power, di = digital in, do = digital out, ldi= low voltage differential digital in, ldo= low voltage differential digital out, ai=analogue in, ao = analogue out, pu = pull-up, pd = pull-down
Low voltage logical = 0V(“1”)/-0.2V(“0”)
Logical = +2V (“1”) / -2V (“0”)

Pads on the second pad-row, listed from upper to lower. These pads are for over-riding of internally generated biases.

Pad name	Type	Description	Nominal value
vfsg	ai	Control voltage for the feedback resistor in the gain stage	~330 mV
obi	Ai	Bias for the discriminators	90 uA (int. gen.)
Mo_bi	ai	Bias for the adress and mgo current sources.	-140 uA(int.gen.)
vref	ao/ai	Reference for the output buffer, internally generated by a dummy slow shaper	~-600 mV
trigwb	ai	Trigger width bias	-12 uA (int. gen.)
shabf	ai	Bias for the fast shaper	65 uA (int. gen.)
vrc	ai	Control voltage for HP -filter resistor (NMOS) in front of discriminator	1.4 V (int. gen.)
preb	ai	Bias for the preamplifiers	500 uA (int. gen.)
shabs	ai	Bias for the slow shaper	22 uA (int. gen.)
ibuf	ai	Bias for the analog output buffer	220 uA (int. gen.)
ref_bias	ai	Bias for threshold DACs	20 uA (int. gen.)

5 Layout

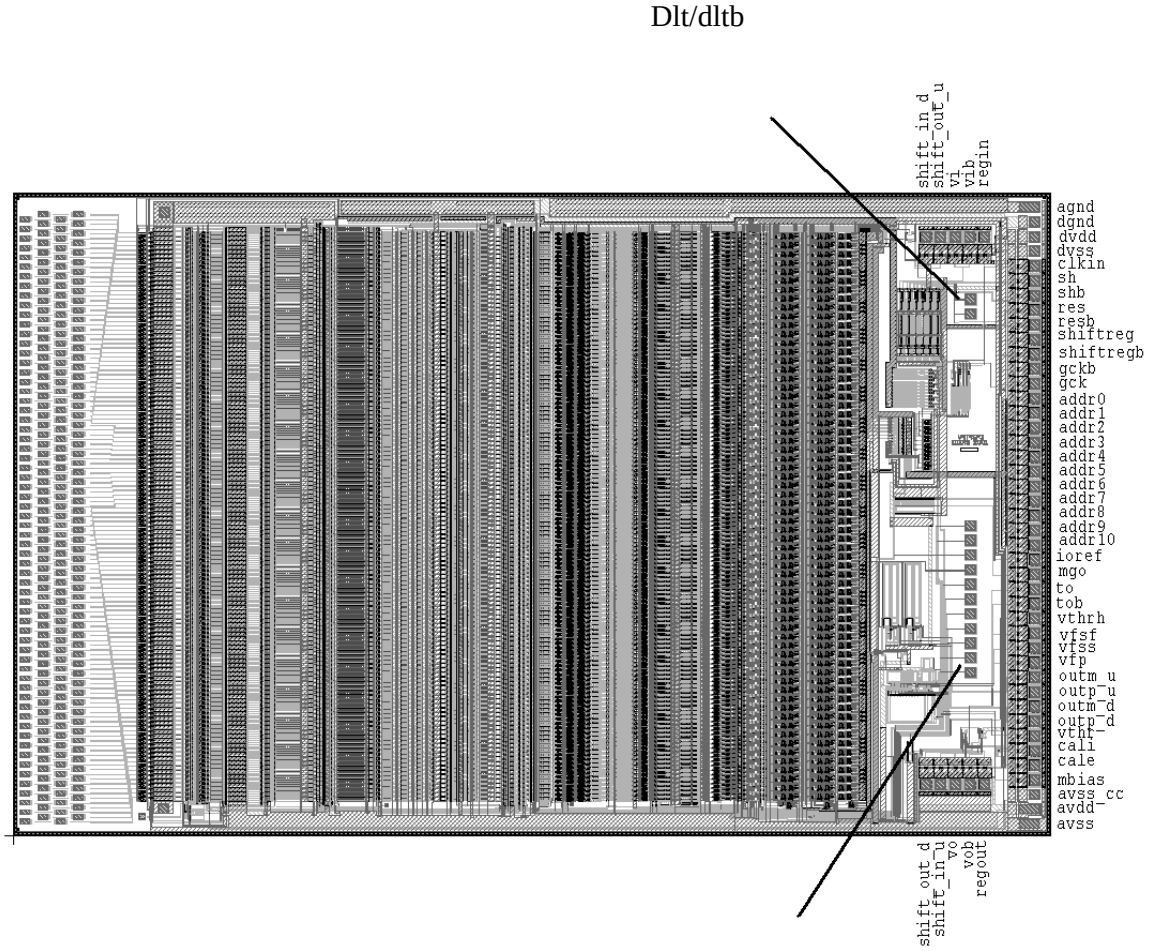


Figure 1: Chip plot of the VaTagp3.

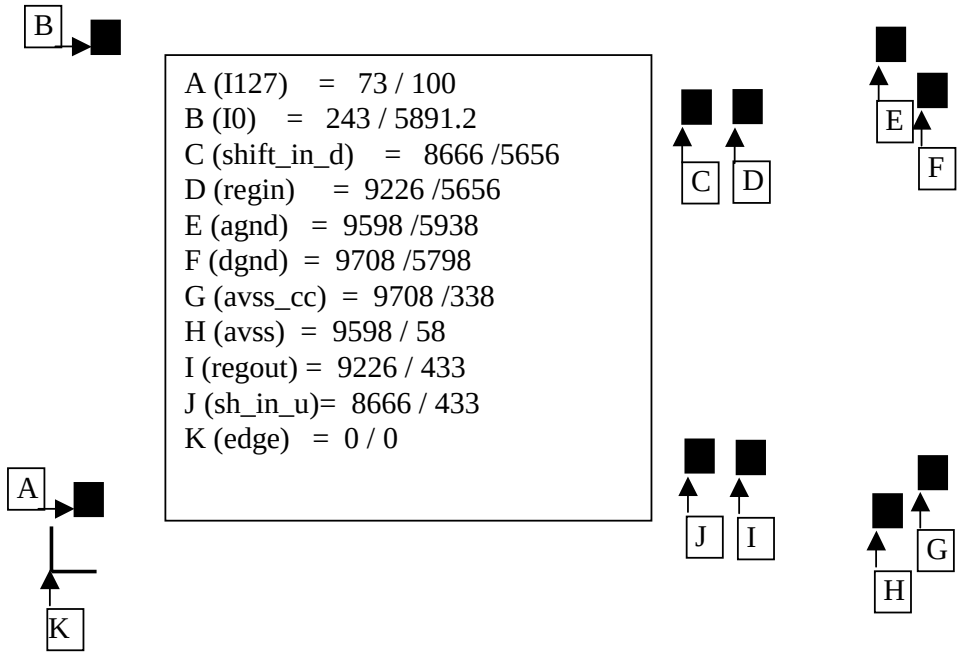


Figure 2: Chip geometry & pad placement (Not to scale - all dimensions in µm. Please note that the referred co-ordinates are layout co-ordinates. Add 50-100 µm on each side for scribe/cutting tolerances).

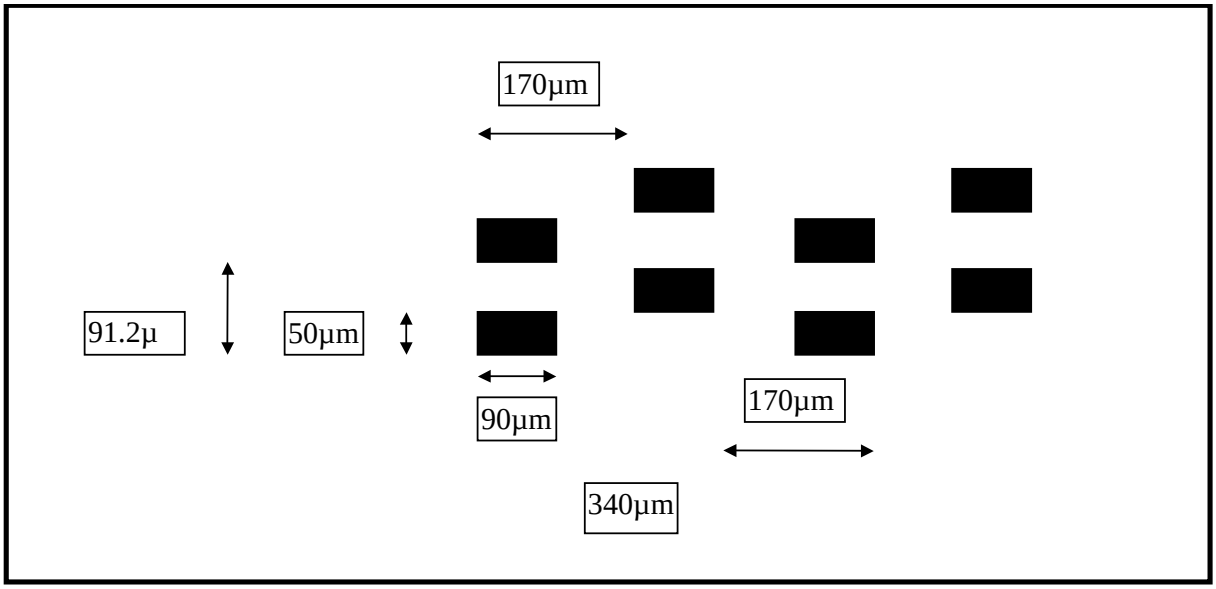
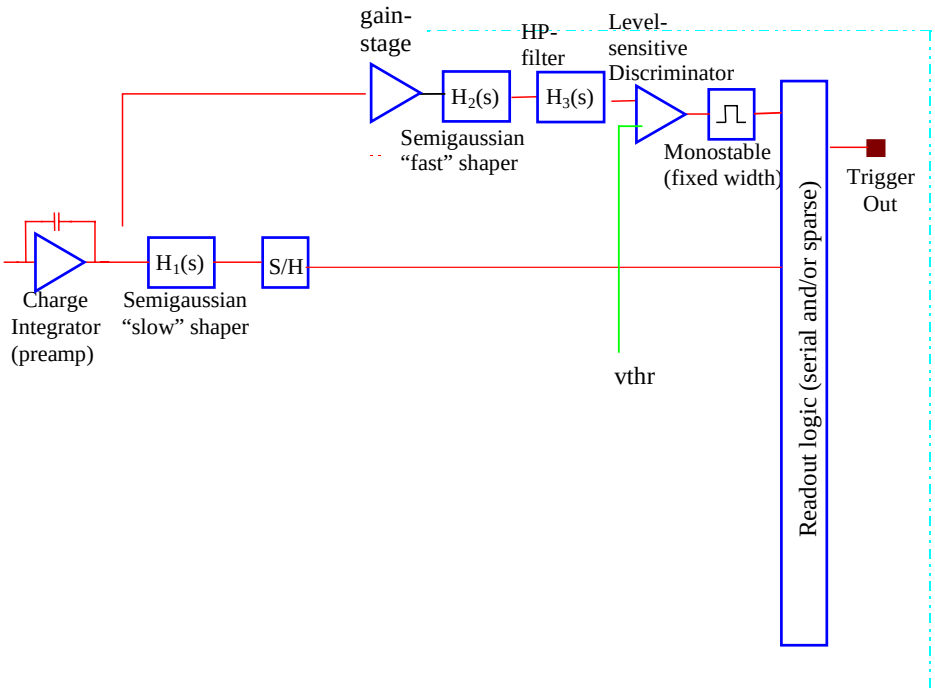


Figure 3: **Definition of input pad size and pitch. Double pad rows are included for redundancy.**

6 Functional description



(see the following text for more detailed information)

6.1 Using VATAGP3 in parallel

The VATAGP2 is designed to be used in parallel for reading out a large number of channels. There are 4 bits for the chip address, giving a maximum of 16 chips on the same bus, with a total of 2048 channels. The pads are placed so that signals that go from one chip to the next are on the opposite side, making the PCB routing easy. The signals should be connected this way: (chip number in parenthesis)

vo(1) to vi(2)
vob(1) to vib(2)
shift_out_u(1) to shift_in_u(0)
shift_out_d(1) to shift_in_d(2)
regout(1) to regin(2)

All other control signals shall be in parallel.

6.2 Biasing

The VATAGP3 is designed to have only one external bias: *mbias*. All other biases are internally generated, where most biases are a fraction of *mbias*. However, sometimes it is necessary to adjust or force the biases to other values than the nominal. Pads are available for all biases so that external adjustment is possible.

Generation of bias currents/voltages

Figure 4 shows a possible approach for generating the necessary bias currents and voltages.

mbias is a current **into** the chip (resistor to VDD).

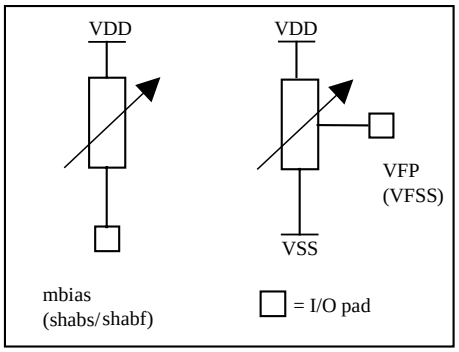


Figure 4: Bias current and voltage generation

Decoupling of power and bias lines

It is recommended to decouple the power and bias lines to GND.

Use 100 nF ceramic capacitors on the power lines as close as possible to each chip and 1-100 uF tantalum capacitors common for all chips on a PCB. Use 100 nF on the *mbias* (and eventually other biases that are externally generated) close to the chip.

6.3 Control register

The VATAGP3 has a 651 bit long control register, set by *regin* and *clkin*.

Bit [1)]	Name	Function
1	cc_enable	Enable current compensation
2	n_side	Current compensation network set for connection to n-side of the detector.
3	test_on	Test mode on
4	select	Select signal polarity
5	bypass	Removes gain-stage from signal path.
6	Gs1	MSB for programmable gain setting.
7	Gs0	LSB for programmable gain setting.
8:11	addr[10:7]	chip address
12:139	Threshold Norm/High for ch[0:127]	Disable channel (assumed that vthrh = +2V/-2V)
140:523	DAC[2:0] for ch[0:127]	Threshold DACs
524:651	test_enable for ch[0:127]	Enable injection of cal-pulse into channel

1) Bit number in the control register. Bit 1 is the first bit after *regin*, bit 648 is the last bit before *regout*. Reverse the order when downloading the bitstream (download bit 648 first and bit 1 last).

The correct use of *Vthr* polarity and select bit setting is shown in the table below, based on the input signal polarity and the *bypass* bit setting:

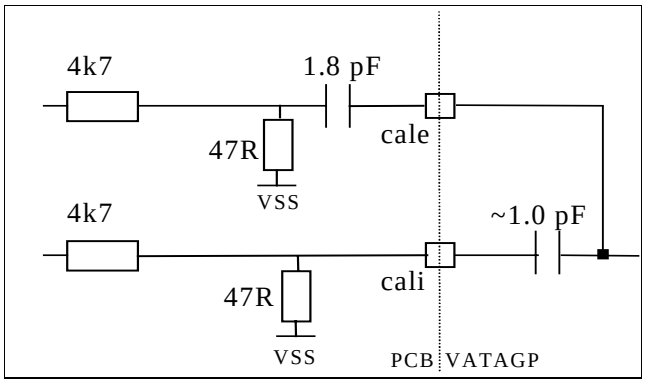
Input signal polarity	BYPASS bit setting	Vthr polarity	Correct SELECT bit setting
Negative	0	Negative	1
Positive	0	Positive	0
Negative	1	Positive	0
Positive	1	Negative	1

6.4 ASIC test and calibration

Each channel can be individually tested. This function is enabled by setting bit *test_on* in the control register to "1". The *test_enable* mask must have one of it's bits set to "1" which will select the corresponding channel (selecting more than one channel is possible due to AC coupling on the inputs but is not expected to be very useful). The channel(s) that has been selected will be sensitive to test-signals injected at the *cale*/*cali* inputs.

Connect **either** the *cali* **or** the *cale* signal. When using the *cale* signal, place the 1.8 pF capacitor is very close to the chip to prevent pickup. When using the *cali* signal, there is a ~1.0 pF capacitor internally in the chip.

A voltage step of 10 mV on the 1.8 pF capacitor gives an input signal charge of 18 fC (~5 MIP).



6.5 Threshold DACs

The DACs have nominally 3 mV step size. The step size can be changed by forcing a different *ref_bi*. The step size in [mV] is **ref_bias[uA]*0.15**.

DAC0	DAC1	DAC2	Threshold adjust (ref_bias=20uA)
0	0	0	0 mV
0	0	1	-3 mV
0	1	0	-6 mV
0	1	1	-9 mV
1	0	0	0 mV
1	0	1	3 mV
1	1	0	6 mV
1	1	1	9 mV

7 Readout modes

The VATAGP3 has three different readout modes. After the physics event, each preamplifier will integrate its eventual signal. The slow shaper will shape the signal with a shaping time of 3 us, and the fast shaper with a shaping time of 1 us. If the signal of the fast shaper has a value larger than the external threshold (*vthr* or *vthr_h*), a trigger on the *to*/*tob* and *mgo* lines occur. When the slow shaper reaches the signal peak (nominally after 3 us), the external hold signal (*sh*/*shb*) should be applied to sample the peak value. Immediately after this, the readout can start.

a) Mode 1: Serial readout

Readout is similar to the VA+TA type of ASICs from Ideas.

A shiftregister will enable readout of one channel at a time. The readout starts with clocking one bit into the first channel of the shiftregister with the *shift_in_d* and *gck*/*gckb* signals. See Figure 4 for an example of the timing in this mode. The logic part of the chip can be reset either by applying the *res/resb*, or by running through the full read-out sequence (more than 128 clocks) so that the last shift bit is clocked out of the register.

On power-up, a reset signal should be applied to reset the internal registers/latches with a pulse (~1us- 1ms) on the *res*/*resb* lines. Eventually, a number of clocks exceeding the number of channels will set the shiftregister to zero.

In this mode, the following input signals are not in use and can be left unconnected:

shift_in_u	(internal pull down)
shift_out_u	
shiftreg	(internal pull up)
shiftregb	(internal pull down)
vi	(internal pull down)
vib	(internal pull up)
dlt	(internal pull down)
dltb	(internal pull up)
vo	
vob	

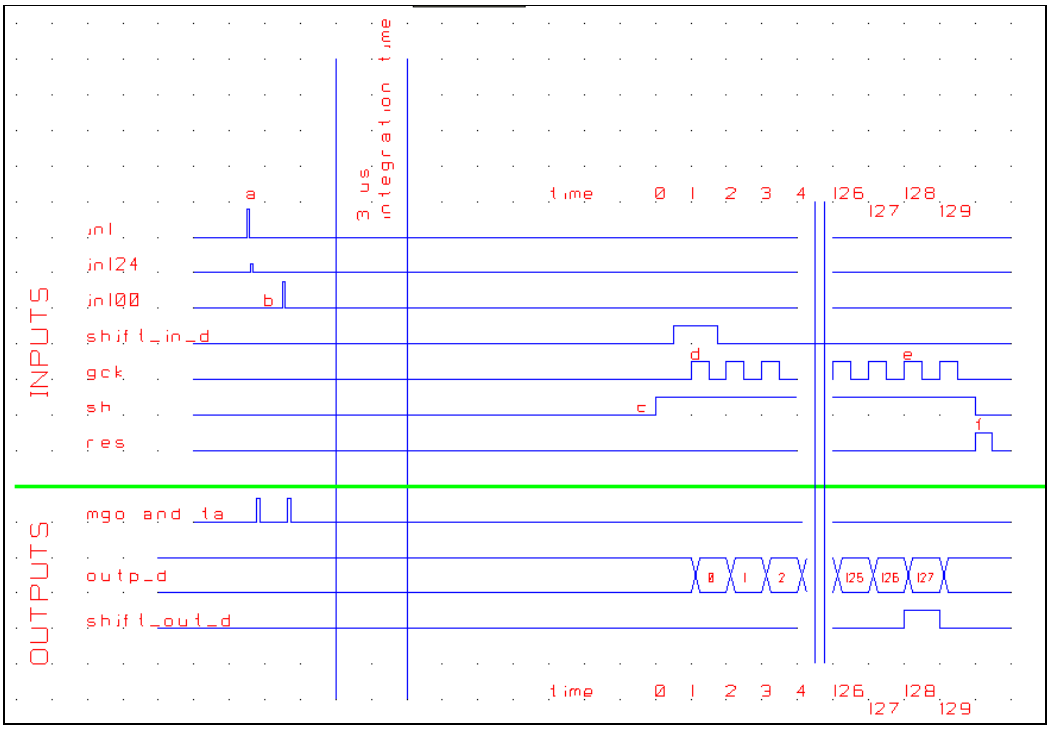


Figure 5: Serial readout

a) Physics events happen almost simultaneously in channel 1 and 124. Since the signal is larger than the threshold, a trigger (*mgo*, *ta*/*tb*) is generated. The fast shaper for the trigger logic has a shaping time of 150 ns, which means that dependent of the signal amplitude and the threshold *vthr*, the trigger can be delayed up to 150 ns.
b) Another physics event happen some time later in channel 100. This event also generate a trigger.
c) After 3 us, the sample-and-hold signal *sh*/*shb* goes high. The signal in channel 1 and 124 have reached the peak, while channel 100 has not fully reached the peak yet.
d) A shift bit is clocked into the shiftregister by *shift_in_d* and *gck/gckb*. The analogue value of channel 0 is enabled at *outp_d/outm_d*. For each clock (*gck/gckb*), the shiftbit is clocked to the next channel.
e) The last channel is enabled. The *shift_out_d* goes high to give a *shift_in* for the next chip in the chain.
f) A reset is applied to reset the shiftregister. This is not necessary if all channels have been clocked, so that the shift bit has been clocked out of the chip.

7.1 Mode 2: Sparse readout

In this readout mode, only the channels with a trigger (signal above the threshold) will be read out to increase the readout speed. As in serial readout, the hold signal *sh/shb* must be applied 3 us after the trigger.

All channels with a trigger will get a read tag. By clocking once with the *gck/gckb*, the analogue value and the address of the first channel with a tag will be available on the output. After the next clock of *gck/gckb*, the next channel with a tag will be available. The *vo* signal goes low when all channels with triggers are read out. If the chip shall be reset before all channels are read out, apply the *res/resb* signal.

In this mode, the following input signals are not in use and can be left unconnected:

shift_in_u	(internal pull down)
shift_out_u	
shift_in_d	(internal pull down)
shift_out_d	

These signals have a fixed level:

vi (chip 0)	connect to VSS (logic low)
vib (chip 0)	connect to VDD (logic high)
shiftreg	connect to VSS (logic low)
shiftregb	connect to VDD (logic high)

dlt/dltb can optionally be used. If they are not used, no connection to these pads are necessary.

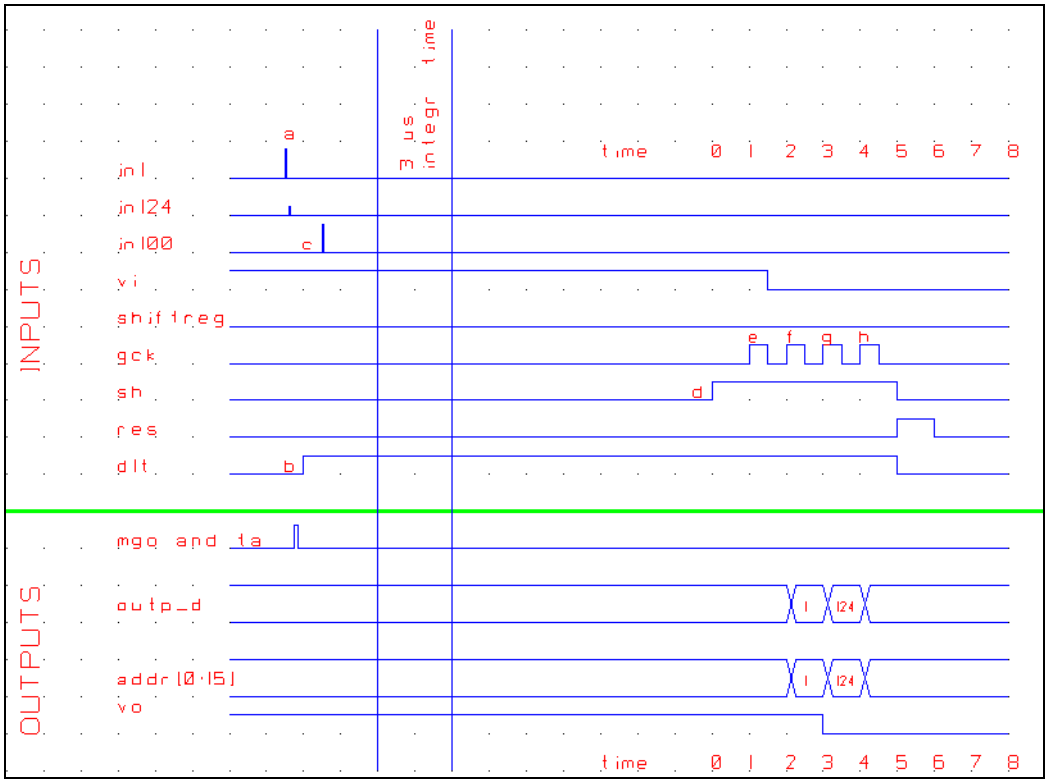


Figure 6: Sparse readout

a) Physics events happen almost simultaneously in channel 1 and 124. Since the signal is larger than the threshold, a trigger (*mgo*, *ta*/*tb*) is generated. The fast shaper for the trigger logic has a shaping time of 200 ns, which means that dependent of the signal amplitude and the threshold, the trigger can be delayed up to 200 ns.
b) The disable_late_trigger *dlt* is applied. This will discard all triggers after this moment. Another physics event happen some time later in channel 100. No trigger is given because *dlt* is high.

c) After 3 us, the sample-and-hold signal *sh*/*shb* goes high. The signal in channel 1 and 124 have reached the peak and are held.
d) The *gck/gckb* clocks once. Since veto in *vi* from the previous chip in the chain is high, no action is taken.
e) The *gck/gckb* clocks once. Veto in *vi* is low, and the first channel with a hit is enabled at the output together with its address.
f) The next and last channel with a hit is enabled at the output together with its address. Veto out *vo* goes low to indicate that all channels are read out and enable readout of the next chip in the chain.
g) *Sh* and *dlt* goes low. A reset is applied to reset the shiftregister by a pulse on *res/resb*. This is not necessary if all hit channels have been clocked, so that the veto out in the last chip has gone low.

7.2 Mode 3: Sparse readout with neighbour channels

This mode is equal to the sparse readout, except that the neighbours of the channel(s) with trigger can also be read out.

As in serial readout, the hold signal *sh/shb* must be applied 3 us after the trigger.

All channels that trigger will get a read tag. By clocking once with the *gck/gckb* and with *shiftreg* low, the analogue value and the address of the first channel with a tag will be available on the output. By setting *shiftreg* high and clocking more clocks, the neighbours of the trigger channel will be available.

Be setting *shiftreg* low and giving another clock of *gck/gckb*, the next channel with a trigger will be available.

All channels with triggers are read out when the *vo* goes low. If the chip shall be reset before all channels are read out, apply the *res/resb* signal.

These signals have a fixed level:

vi (chip 0)	connect to VSS (logic low)
vib (chip 0)	connect to VDD (logic high)

dlt/dltb can optionally be used. If they are not used, no connection to these pads are necessary.

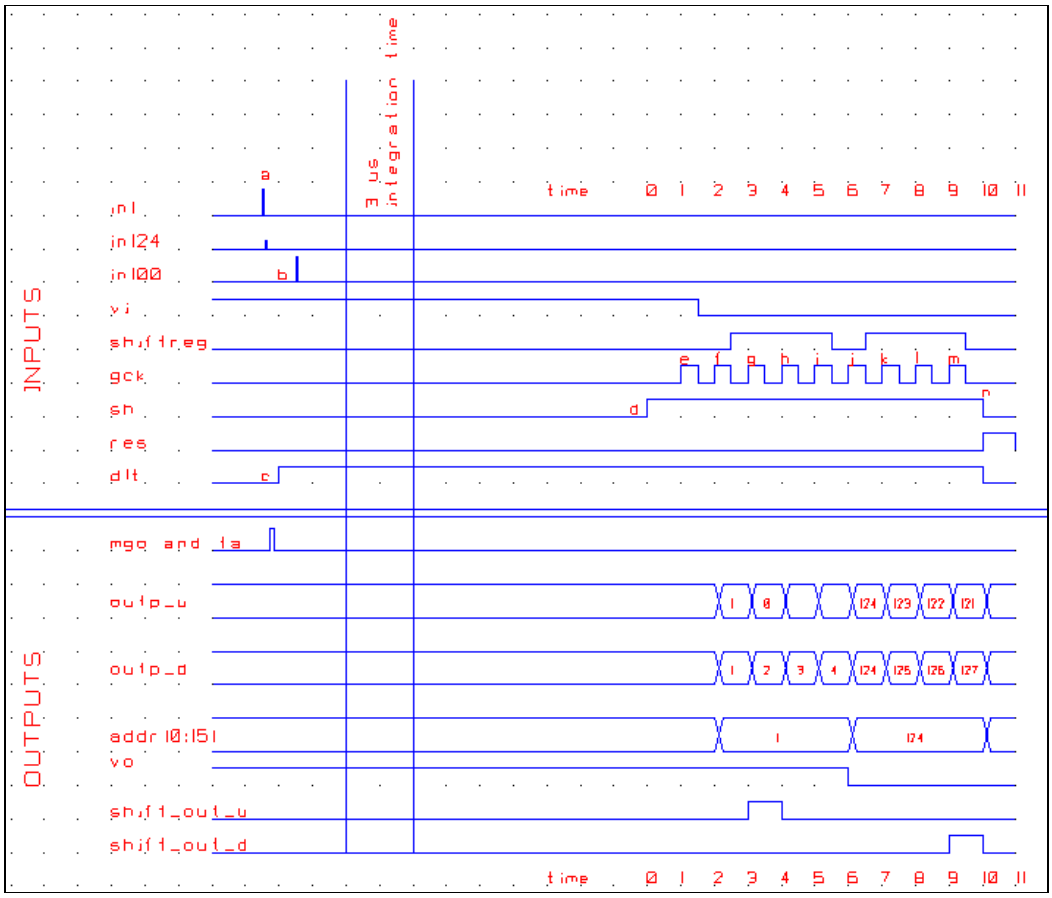


Figure 7: Sparse readout with neighbour channels

a) Physics events happen almost simultaneously in channel 1 and 124. Since the signal is larger than the threshold, a trigger (*mgo*, *ta*/*tb*) is generated. The fast shaper for the trigger logic has a shaping time of 150 ns, which means that dependent of the signal amplitude and the threshold, the trigger can be delayed up to 150 ns.
b) The disable_late_trigger *dlt* is applied. This will discard all triggers after this moment.
c) Another physics event happen some time later in channel 100. No trigger is given because *dlt* is high.
d) After 3 us, the sample-and-hold signal *sh/shb* goes high. The signal in channel 1 and 124 have reached the peak and are held.
e) The *gck/gckb* clocks once. Since veto in *vi* from the previous chip in the chain is high, no action is taken.
f) The *gck/gckb* clocks once with *shiftreg* = low. Veto in *vi* is low, and the first channel with a hit is enabled at the output together with its address.
g) The *gck/gckb* clocks once with *shiftreg* = high. The analogue values of the two next neighbour channels of the hit channel are read out on the *outp_u/outm_u* and *outp_d/outm_d* lines.
h) Same as g)
i) Same as g)
j) The *gck/gckb* clocks with *shiftreg* = low. The next channel with a hit is enabled at the output together with its address.
k) Same as g)

l) Same as g)
m) Same as g)
n) The chip is reset by setting *sh* and *dlt* low and by giving a short *res/resb* pulse. *Dlt* is not available on this ASIC.

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