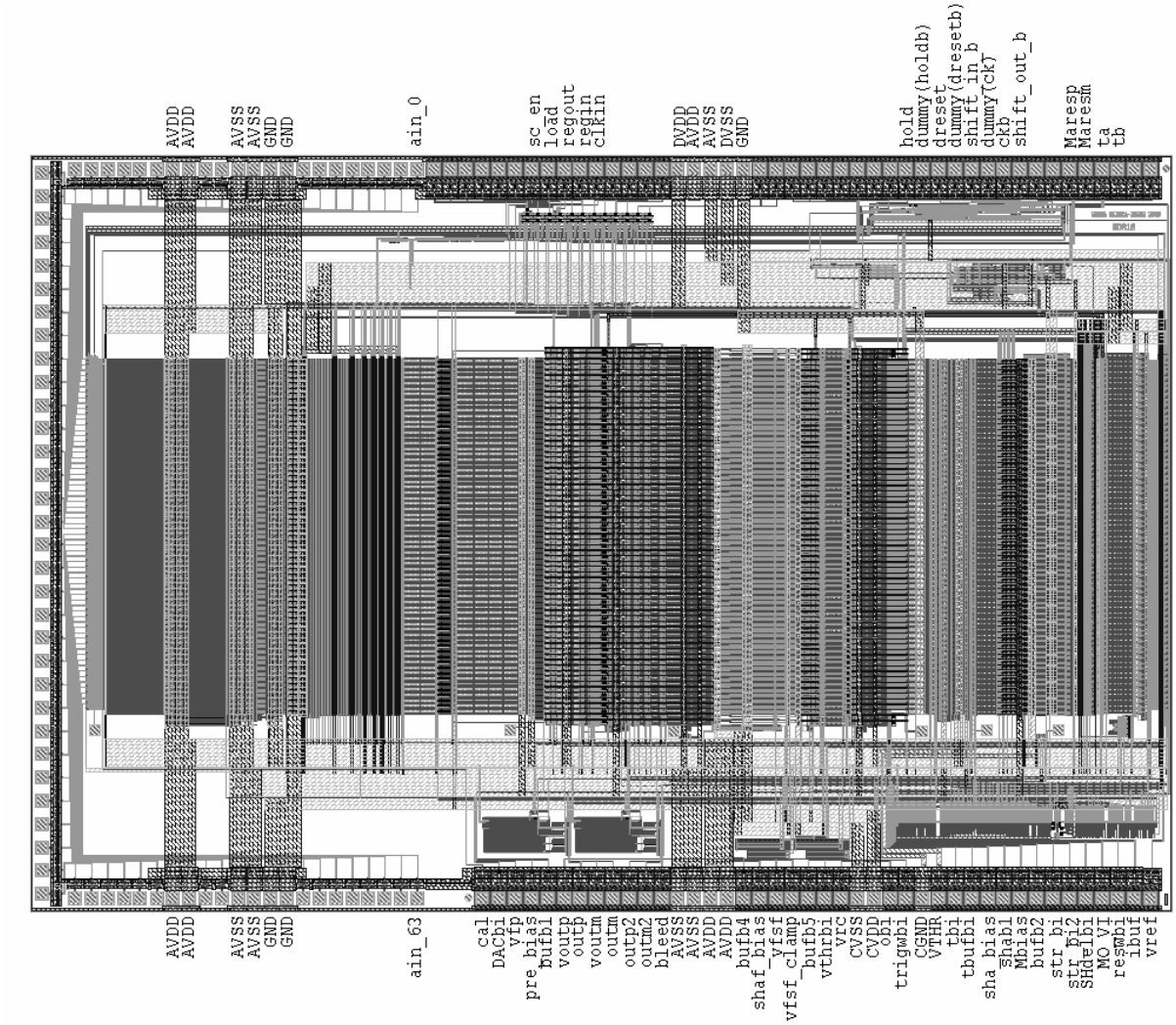
VATA64HDR16



SPECIFICATION V2R1

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1 Specifications

The VATAHDR16 is an ASIC optimized for energy and timing measurements with Silicon Photo Multiplier (SiPM) detectors. It is based on a combination of the existing ASICs VA32_HDR14.2 and a TA32cg. The functionality of these ASICs has been complemented with new functionality tailored for SiPM read-out.

1.1 General

Parameter	Value	Comment
Number of channels	64	
Channel architecture	VA-TA	Spectroscopic energy measurement output, Trigger output, and trigger timing measurement (Time-to-analog) output. The ASIC can be configured to generate the Sample-and-hold (SH) signal by itself.
Connection to detector	DC	Project goal

1.2 Performance

The following parameters are based on preliminary analyses. The outcome of the deisgn phase will be an updated performance table. Where nothing else is stated, the parameters are given for the main ASIC configuration.

Parameter	Typical value	Description, Comment
Peaking time: ➢ Slow shaper ➢ Fast shaper	 100ns 50ns	Adjustable. Optimized for typical scintillator LYSO. In addition, there will be settings for programming the slow shaper, e.g. four settings 50/100/150/300ns (TBD).
DNR	~20/55pC	With default settings and voltage output, up to 20pC can be achieved. With alternative gain settings, up to 55pC can be achieved. Please note that the linearity will be degraded at 20pC (like for the VA32HDR14.2). Good linearity for the HDR14.2 (current output) is achieved for charges below 10-12pC.

Parameter	Typical value	Description, Comment
Charge polarity	positive	Both positive and negative charge. Please observe that the ASIC is optimized for positive charges. Some of the ASIC functionality may only be available for positive charges.
Detector capacitance	<200pF	Noise analysis, peaking time ranges and power estimates are based on a lower input capacitance. It will be checked how the ASIC performs for loads up to 500pF, but this will not be the main facos of the design work.
Detector leakage current	Up to 10µA.	The detector DC leakage current is assumed to be very low. For SiPM, the dark count rate can make the effective leakage current reach the 10µA.level.
Noise	~1.2-1.6fC	
Dynamic range (before saturation), voltage output	~20 pC	Positive charge, using the voltage output buffer.
Dynamic range (before saturation), voltage output, low gain setting	~55pC	Positive charge, using the voltage output buffer.
Time measurement output • Range: • Gain:	 ~1.8µs ~0.8mA/µs	

1.3 Power supplies

Please be aware that ASIC performance may change outside the default power supply settings.

Parameter	Conditions	Value	Units	Comment
Supply voltage, AVDD Supply voltage, AVSS		+2.5 -2.5	V (typ) V (typ)	Ref. AGND Ref. AGND
Supply voltage, AGND		0		
Supply voltage, DVDD Supply voltage, DVSS		+2.5 -2.5	V (typ) V (typ)	Ref. AGND, should not be higher than AVDD Ref. AGND, should not be lower than AVSS

Parameter	Conditions	Value	Units	Comment
Stress ratings power supply		5.5	V (max)	Absolute max rating between AVSS and AVDD.
Allowed voltage range, I/O pins		AVSS AVDD	V(min) V(max)	To prevent Latch-up and ESD damage
Back contact		AVSS	V (typ)	The back contact should preferably be connected to AVSS
Power dissipation		TBD	mW (typ)	Quiescent, ASIC total. Some stages that may not be used in all modes will have independent power down options.

1.4 Output and Interface

Parameter	Conditions	Value	Units	Comment
Readout clock rate		10	MHz (max)	Not for required noise performance
Logic input low		-1.5	V (max)	
Logic input high		+1.5	V (min)	
Logic output low		-2.3	V (max)	
Logic output high		+2.3	V (min)	

1.5 Mechanical and Process

The figures given for the Human Body Model are typical values, but have not necessarily been measured for all pins.

Parameter	Conditions	Value	Units	Comment
Manufacturing process		0.35	µm	CMOS, epitaxial layer
Die size, length	Not including scribe.	9.81	mm	From preamplifier inputs to opposite side
Die size, width	Not including scribe.	6.5	mm	
Thickness		450	µm (typ)	
Bonding pad pitch		140/200 140	µm µm	Preamplifier input pads Control, output, bias, and power pads
Bonding pad size		100 x 75 90 x 90	µm µm	Preamplifier input pads Control, output, bias, and power pads
Bonding pad series resistance		0 0/500	Ω Ω	Preamplifier input pads Control, output, bias, and power pads
Bonding pad ESD protection	Measured by the Human Body Model.	>2000	V (typ)	Preamplifier input pads, protection diodes. Control, output, bias, and power pads

2 Detailed Description

An overview of the ASIC can be found in Figure 1. It shows the connection of the Front-End (described in section 2.1), the Back-End (see section 2.2) and the calibration circuitry (section 2.3). The external signal *holdb* is used to sample all channels for serial read-out. Serial read-out is done with the Back-End circuitry and the differential current output buffer. The output buffer reference voltage *vref* is generated by an unconnected channel (the "dummy channel").

The analog output buffers will have either current or voltage output. This can be selected in the slow control configuration register.

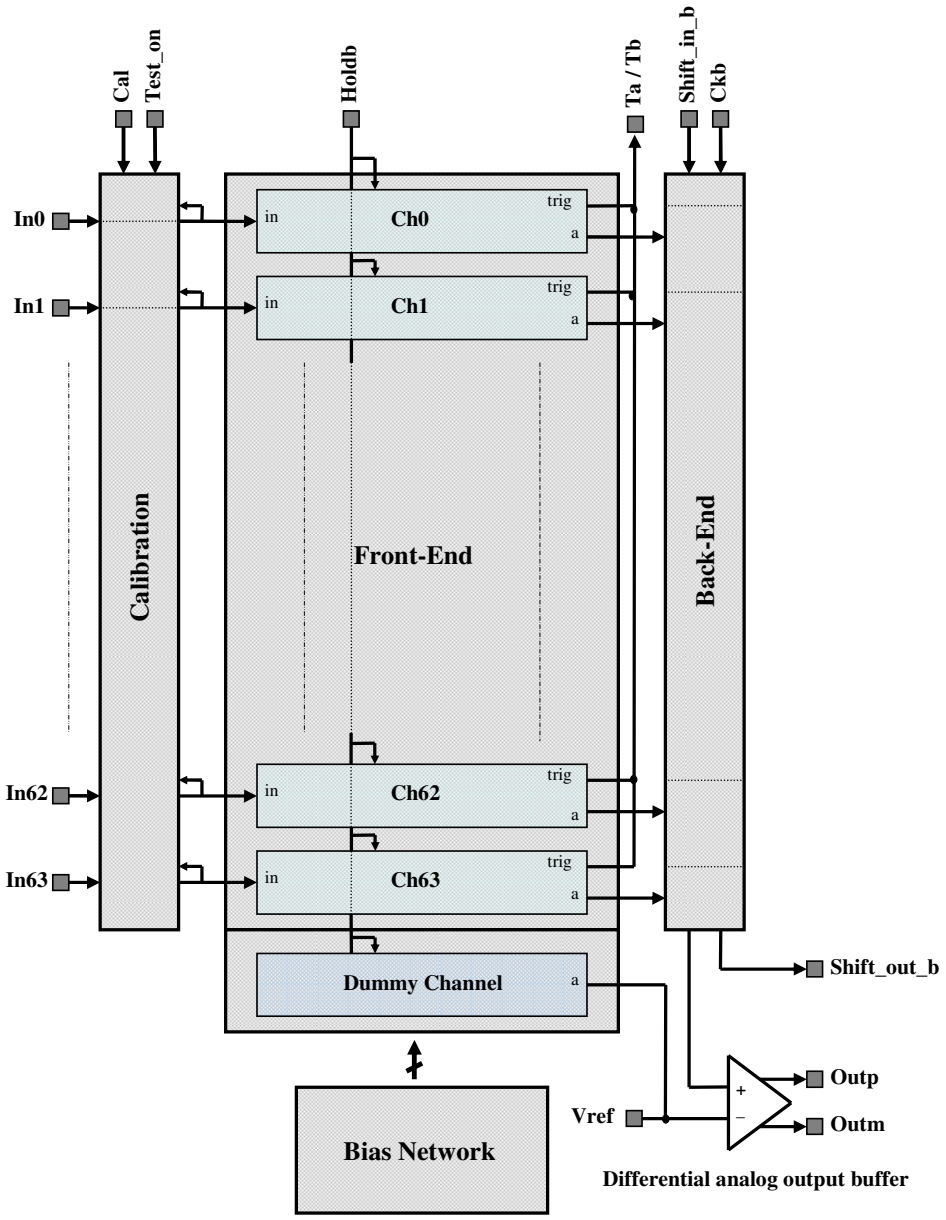

Figure 1: Top level diagram for he VATAHDR16. The analog signal processing is done in the Front-End channels, while the read-out is handled by the Back-End. The Front-End consists of 64 amplifier channels.

2.1 ASIC Front-End

The analog signal processing is done in the Front-End channels. The architecture of the channels is shown in Figure 2. Each channel consists of a charge sensitive preamplifier, a signal processing branch for measuring the pulse height (energy) and another branch for triggering and timing measurement.

The energy measurement branch consists of a first order semi-Gaussian CR-RC noise filter ("Slow Shaper"), a peak-hold device and a Sample-and-Hold unit.

In normal mode of operation the 64 inputs are connected to a detector that generates charge signals. After a physics event in the detector, each channel will integrate any deposited charge. To sample the measured energy, an external or internal *SH* signal should be applied when the

slow-shaper reach the peak (~100-200ns). The sampled value can be accessed through the read-out circuitry in the Back-End (see section2.2). The ASIC can be configured to either sample the slow shaper output directly, or to sample the output of the peak-hold device.

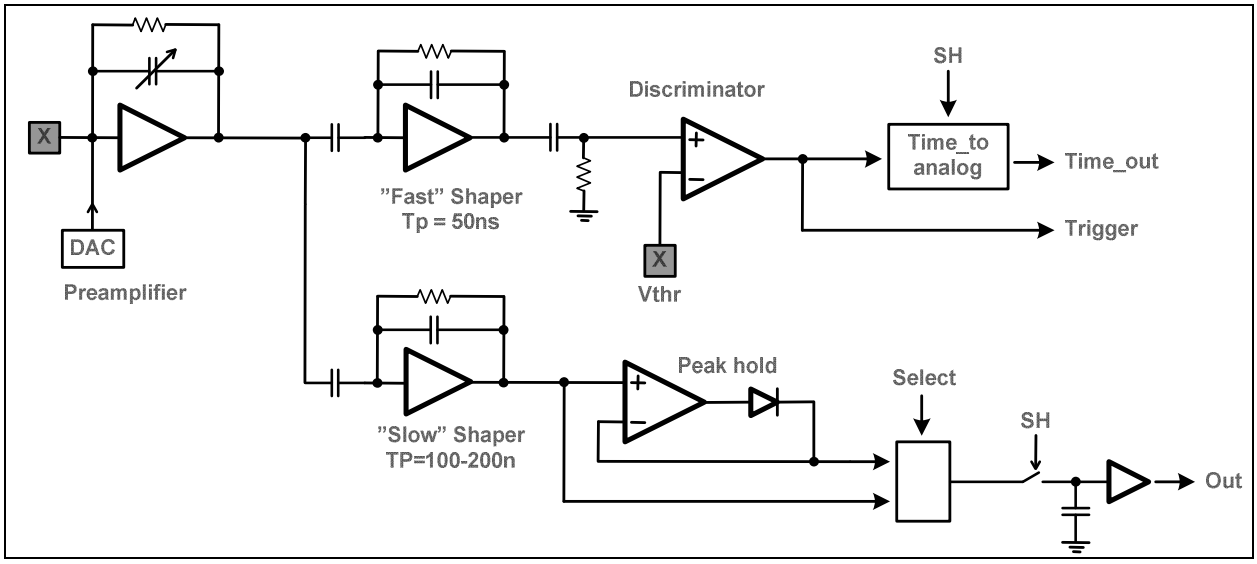

Figure 2: A block diagram of the ASIC channel. The channel consists of a preamplifier, a fast shaper for trigger generation and a slow shaper for energy measurement. The output of the shaper goes to a discriminator. The trigger is used to derive the on-chip Sample and hold signal, as well as a time measurement signal in the time-to-analog converter. The slow shaper is followed by a peak hold device. The peak hold device can be bypassed by setting a slow control configuration bit (i.e., normal VA-operation).

The trigger processing branch consists of a fast shaper (with a typical Tp of 50ns), a discriminator and a Time-to-Analog-Converter (TAC). If the channel detects a signal above the threshold, it will output the trigger to the ASIC Back-End. The trigger will be output to the global off-chip trigger line, and may also be used to generate an on-chip SH signal. The TAC consists of a voltage ramp that begins upon the trigger and is sampled with the SH signal. The output of the TAC unit in all channels will be output serially on a separate current output buffer (ASIC pins outp2/outm2).

If the peak hold device and/or the TAC unit are used, the ASIC must be reset with the MARES signal after each signal acquisition. This is not necessary in case sampling of the slow shaper and only the TA trigger is being used.

2.2 ASIC Back-End

The read-out circuitry located in the Back-End of the ASIC is described in Figure 3. The outputs *a* of all channels is connected to the inputs of a 64 channel multiplexer. The switches in the multiplexer are controlled by a bit-register, and can be used to read out all channels serially. There are two output multiplexers running in parallel, one for the sampled slow shaper energy measurement and one for the TAC values.

The output of the multiplexer goes directly out of the chip via the differential output buffer (*signal* = ***outp*** - ***outm***). Only one of the switches in the multiplexer can be ¨on ¨ simultaneously.

Thus, only one channel can be seen at a time on the ASIC output. The bit in the register is clocked sequentially from the first to the last channel by clocking *ckb*. The clock can be stopped at any point, which will leave the connection between the current channel and the output.

There are two parallel analog outputs; for the TAC-values, and for the slow shaper outputs.

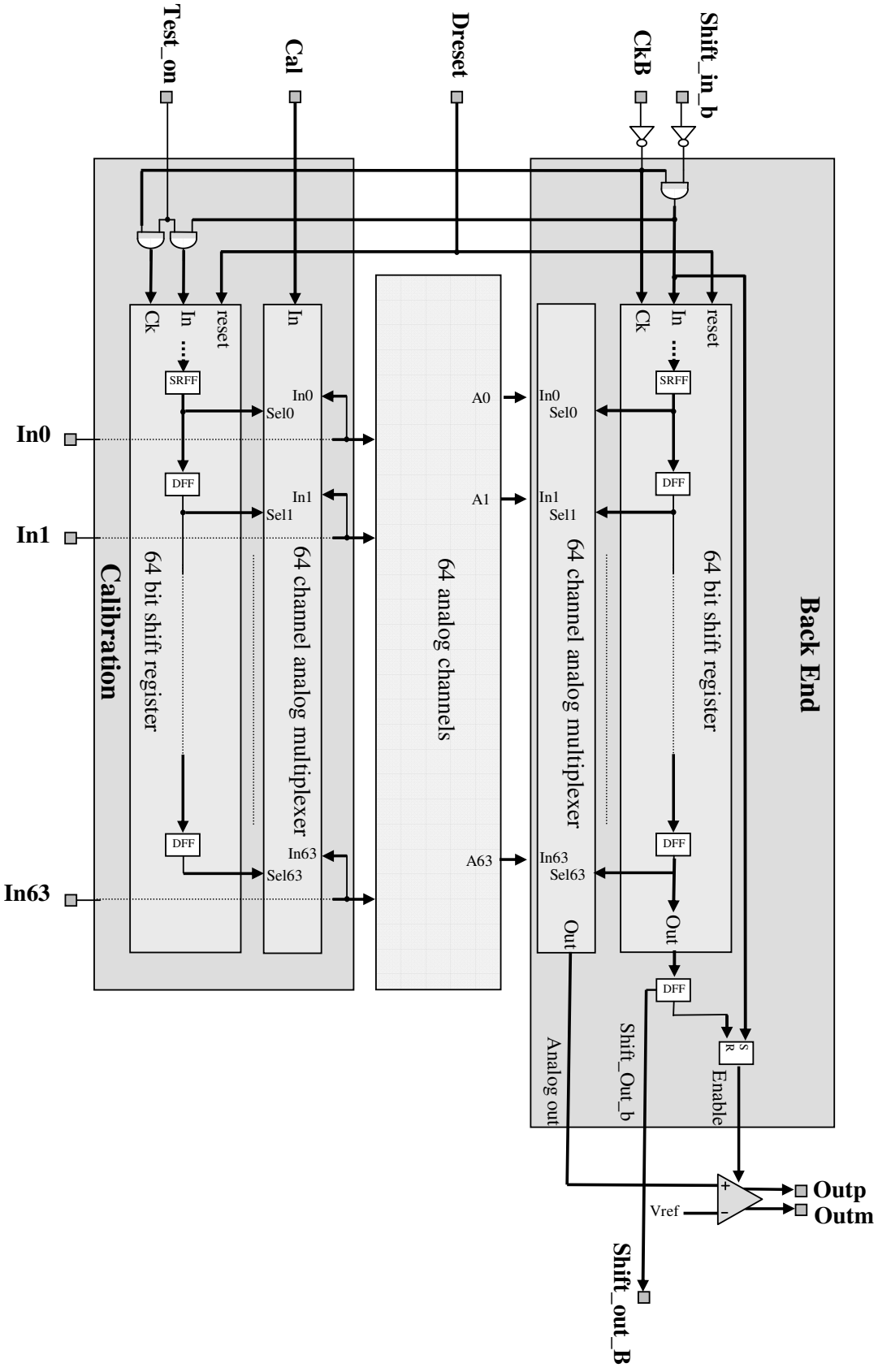

Figure 3: To be updated. Overview of the ASIC Back End and Calibration circuitry. The calibration circuitry is described in section 2.3). Please be aware that there are two multiplexers and two output buffers; one for the sampled slow shaper outputs and one for the outputs of the TAC units.

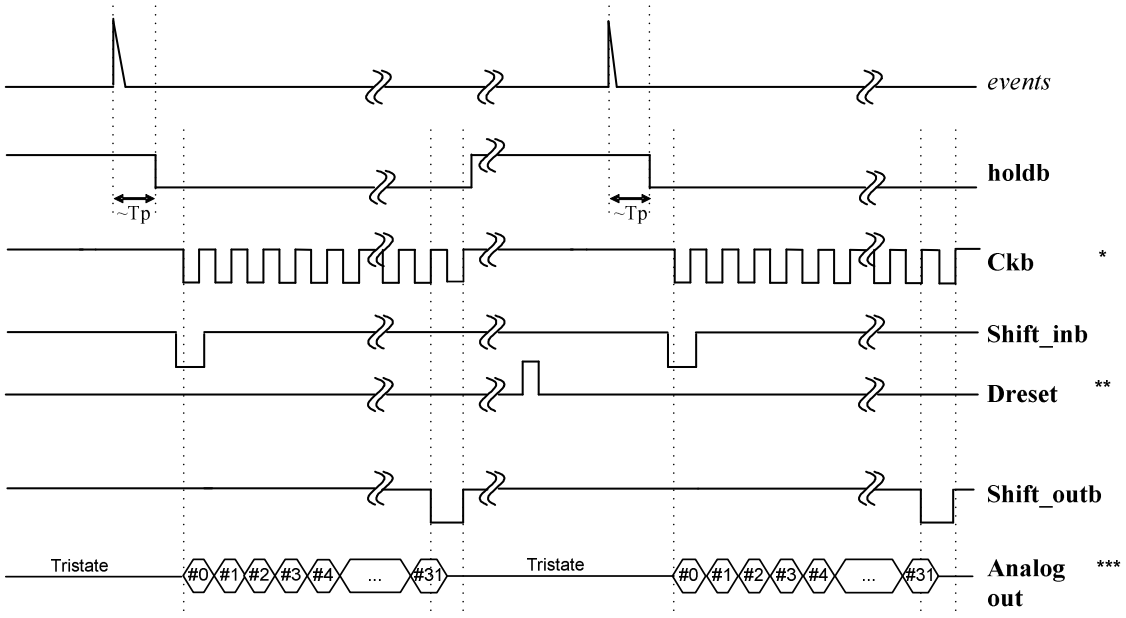

Figure 4: Timing diagram for readout of the VATAHDR16. The cycle starts with the occurrence of the event. After the event, holdb is applied one peaking time after the event, to sample and hold the shapers at the peak. The asic is ready to be clocked out 100ns after a hold is applied. The readout is initiated by clocking (Ckb) a one into the shift register (shift_inb). If all channels are read out one do not need to apply the digital reset (dreset). "mares" is not shown in the timing diagram, but must be used in case the peak-hold device or the TAC–unit are used.

The timing diagram for a normal read-out sequence is shown in Figure 4. The list of the important timing values is shown in Table 1. After the physics event, each channel will integrate and filter the charge for a time given by the slow shaper peaking time Tp. Each channel has a peak-hold device that will find the peak of the slow shaper signal. If the peak hold is being used, the sampling time does not have to be aligned with the peaking time.

The fast shaper and discriminator in each channel will produce a trigger when the charge is above the global threshold voltage. Each channel has a 4 bit trim DAC to remove threshold offsets. The trigger will be available on the external pads ta/tb to flag the event, and will also be used internally in the ASIC to turn on the peak-hold devices and to generate the internally generated sample and hold signal *holdb*(also available on an external pad). If the TAC option is implemented, this signal will also be used to generate the timing.

The *holdb* signal will be applied to sample all channels. The sequential read-out of the channels can be started by activating the output bit-register using overlapping *shift_in_b* and *ckb* signals. The analog data from channel 0 will appear on the output after the first negative flank of *ckb*. The analog output buffer will be tri-stated prior to the read-out, and will be activated simultaneously with the appearance of the data of channel 0. The settling time for the analog output might therefore be slightly worse than for the other channels. Typical maximum clock frequency is 10MHz, but this is only possible with a good external receiver and low load.

The *holdb* signal may be generated internally, please refer to section 2.2.1. If the internal SH generation is used, a dreset must be applied after read-out to reset the *holdb* signal.

The serial read-out of the ASIC has been designed for daisy-chaining several ASICs on the same output bus. This is achieved by connecting the output signal of the first ASIC's shift

register (*shift_out_b*) to the next ASIC's *shift_in_b* pad. The *shift_out_b* signal from the first ASIC will appear after the positive edge of *ckb* during the data output of the last channel. The next negative transition of *ckb* will enable the next ASIC's read-out circuitry.

After read-out, the system should issue the *mares* signal if the ASIC uses the peak hold devices or the TAC unit.

Signals (listed in chronologic sequence)	Signal delay		Signal hold time	
	Delay	Related to which signal	Delay	Related to which signal
Event	-	-	-	-
Holdb	Tp	1st event	100ns	Last Ckb
Shift_inb	200ns	Holdb	100ns	First Ckb
Ckb	100ns	Shift_inb	-	-

Table 1: List of critical timing values at ASIC pins.

2.2.1 Sample and Hold generation

The ASIC can be sampled in three different ways:

1. External sampling through the pads *hold* / *holdb*. This is the normal VA sampling method.
2. Internally generated sampling based on an internal trigger in the ASIC. To enable this, please set the slow control bit *SH_gen* high. The SH signal will now be issued at a time delay set by the holdbi bias.
3. Internally generated sampling based on an external trigger. To enable this, please set the slow control bit *SH_sense* high. The ASIC will sense the *TA/TB* lines to see if any other ASIC has triggered. The SH signal will be issued at a time delay set by the holdbi bias.

Any combination of the three modes can be used. A dreset must be applied after read-out to reset the *holdb* signal when using internal generation of SH.

2.3 Initialisation

The ASIC will always be in an initialized state after *dreset* is applied, or after a normal read-out sequence without *dreset*. The ASIC will also need a down load of the slow control configuration register after power-up. If the peak hold devices or the TAC unit is used, the system should also issue a mares signal to initialize the ASIC.

2.4 Test and Calibration

Each channel can be tested individually without connecting the input. This can be done by enabling the calibration circuitry (described in Figure 3) with the *test_on* configuration bit. In addition, the individual test bit for the channel to be tested must be set high. When both these bits are high, the preamplifier input is connected to the *cal* signal. The timing diagram for the test mode is equal to normal read-out, refer to Figure 4 for details. As for the read-out described in

section 2.2, only one connection at a time is possible. This connection corresponds to the same channel that is connected to the output buffer.

When using the cal signal, place a capacitor very close to the ASIC to prevent pickup. Apply a voltage step to inject a calibration charge. A voltage step of 100 mV on a 47pF capacitor gives an input signal charge of 4.7 pC. Some additional noise due to routing and coupling of signals has to be taken into account when operating the ASIC with calibration pulses.

2.5 Slow control serial configuration register

The ASIC "slow control" configuration register contains bits for configuration and calibration. The register file is a serial shift register with a read-back option. Data should be applied to the "reg_in" pad, clocked in by "clk_in", and can be read back through the "reg_out" pad. Default value of the bits is '0'. A timing diagram for the slow-control configuration can be found in Figure 5.

In order to update the contents of the preamplifier input DACs, the external *load* signal should be pulsed. This is not necessary in case the preamp DACs are disabled.

This register file must be downloaded into the ASIC after power-on. The register is volatile and configuration data is lost when power is off.

The contents of the serial configuration register are shown in Table 2.

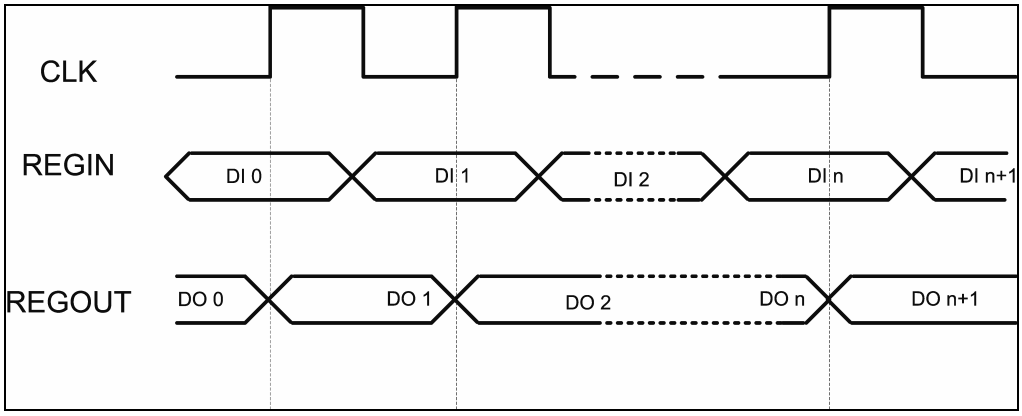

Figure 5: Timing diagram for the operation of the ASIC serial configuration register. Please be aware that the load signal should be pulsed after register loading is done in order to update the preamplifier input potential DACs.

To configure the serial slow control register, the ASIC can either use the serial loading described above, or use external overriding of the bits. The external overriding is available for bit 0-22 (see Table 2). The table lists the bits in sequence from the regin pin. When down loading the bits, bit 0 should be the last bit in the bit stream.

In order to use the external bit setting (e.g. in critical space applications), the external pin *SC_en* must be bonded to DVSS. The pad has an internal 10kohm resistor to DVDD. This will override any contents in the flip-flops of bit0-22. All of these bits are then pulled to logic low. To

set any of the bits, bond the corresponding *SC_ext* –pad found in Table 2 to DVDD, all of these pads have an internal 10kohm pull resistor to DVSS.

Bit #	bits	Ext. pad	Name	Description, comment
0		Sc_ext0	Dac_on	Enable the preamplifier input potential DAC. If this bit is 0, the content of the preamplifier input potential DACs is 'don't care'.
1		Sc_ext1	Lg	Set high to set the preamplifier in low gain mode.
2		Sc_ext2	Rfp_bp	Set the bit high to increase the preamplifier feedback resistance.
3		Sc_ext3	Rfs0_b	Set this bit high to increase the shaper feedback resistance. LSB
4		Sc_ext4	Rfs1	Set this bit high to decrease the shaper feedback resistance.
5		Sc_ext5	Rfs2_b	Set this bit high to increase the shaper feedback resistance. MSB
6		Sc_ext6	Lgs	Set this bit high to set the slow shaper in low gain mode.
7		Sc_ext7	Ssc0_b	Set this bit high to decrease the slow shaper output load. LSB
8		Sc_ext8	Ssc1	Set this bit high to increase the slow shaper output load.
9		Sc_ext9	Ssc2	Set this bit high to increase the slow shaper output load. MSB
10		Sc_ext10	Tp50_dc	Set this bit high to optimize DNR for slow shaper TP=50ns
11		Sc_ext11	Bypass	Set this bit high to bypass the peak hold device and use VA-style peak sampling in stead.
12		Sc_ext12	Sel	Set this bit high to configure trigger logic for negative charges.
13		Sc_ext13	Shabi_hp1b	Set this bit high to decrease the slow shaper bias current. LSB
14		Sc_ext14	Shabi_hp2	Set this bit high to increase the slow shaper bias current. LSB
15		Sc_ext15	Shabi_hp3b	Set this bit high to decrease the slow shaper bias current. MSB
16		Sc_ext16	SHsense_en	Enable internal SH generation based on external trigger on the *Ta/Tb* line. The SH delay is determined by the bias *Holdbi*.
17		Sc_ext17	SHgen_en	Enable the internal SH generation based on internal trigger. The SH delay is determined by the bias *Holdbi*.
18		Sc_ext18	Buf_sel	Set this bit high to use the current output buffer for the serial energy output.
19		Sc_ext19	Test_on	Set this bit high when testing the ASIC with the external *cal* signal.
20		Sc_ext20	Vfp_en	Set this bit high to enable the *vfp* bias (by default disabled).
21		Sc_ext21	Vfsfclamp_en	Set this bit to enable the fast shaper saturation recovery circuit.

Bit #	bits	Ext. pad	Name	Description, comment
22-23	2	Sc_ext22	reserved	Reserved for future use.
-87	64		Disable register	One bit for each of the 64 channels [ch0,…ch64]
88			Disable bit tst channel	Disable bit for the test channel
-344	256		Threshold alignment DAC	For aligning the threshold voltages for all channels. Each channel has a 4 bit DAC , [ch0[bit0, …bit3], … ch63[bit0, …bit3]] Bit0 is LSB, bit2 is MSB, bit 3 is the sign bit.
-348	4		Threshold alignment DAC tst channel	4 bit for threshold alignment, [bit0, …bit3] Bit0 is LSB, bit2 is MSB, bit 3 is the sign bit.
-860	512		Preamplifier input potential DAC	8 bit DAC in each channel for tuning the input potential of the preamplifier. [ch0[bit0, …bit7], … ch63[bit0, …bit7]]. Bit0 is MSB, bit7 is LSB.
-868	8		Preamplifier input potential DAC, tst channel	8 bit DAC for tuning the input potential of the preamplifier. [bit0, …bit7], Bit0 is MSB, bit7 is LSB.
-872	4		Holdbi Bias DAC	4 bit bias DAC for tuning the hold delay bias Holdbi. [bit0, …bit3], Bit0 is LSB, bit2 is MSB, bit 3 is the sign bit.

Table 2: Overview of the slow control serial configuration register, listed in sequence from the regin pin. Bit # 872 should be the first bit in the bit stream, since it is located at the end of the register chain.

Bit3	Bit2	Bit1	Bit0	Bias (µA)	Hold delay (ns)
0	0	0	0	Default: 10uA	250
0	0	0	1	20	125
0	0	1	0	30	83
0	0	1	1	40	63
0	1	0	0	50	50
0	1	0	1	60	38
0	1	1	0	70	36
0	1	1	1	80	31
1	0	0	0	Default	250
1	0	0	1	9	278
1	0	1	0	8	313
1	0	1	1	7	357
1	1	0	0	6	375
1	1	0	1	5	500
1	1	1	0	4	625
1	1	1	1	3	830

Table 3: Hold delay as a function of bits in the Holdbi DAC

Bit	Tp=50ns	Tp=100ns	Tp=150ns	Tp=300ns	Tp=100ns, Half gain
Rfs0_b	1	0	0	0	0
Rfs1	1	0	0	0	0
Rfs2_b	0	0	0	1	0
Ssc0_b	1	0	1	0	0
Ssc1	0	0	1	0	1
Ssc2	0	0	0	1	0
Tp50_dc	1	0	0	0	0
Shabi_hp1b	0	0	0	1	1
Shabi_hp2	1	0	1	0	1
Shabi_hp3b	0	0	1	1	1
lgs	0	0	0	0	1

2.6 ASIC Pin Description

The pins of the VATA64HDR16 are listed below. This is to be updated. The Va32_HDR14.2 has a total of 45 pins, in addition to the 32 input pads. Not all of them will need connection in the system. In Table 4, the output, control and power pads are listed clockwise from the upper left corner. Positive current direction is into the chip. All voltages assume an ASIC powered with typical values of VDD and VSS as described in the table.

Pad name	Type	Description	Nominal value	Typ. V (cur. Biases)	Max V. (mV)	Min V. (mV)
Ain_15	ai	Analog input to channel 15				
..						
avdd	p	Analogue vdd. 2 pads.	+2.5 V			
avss	p	Analogue vss. 2 pads.	-2.5 V			
gnd	p	signal ground. 2 pads.	0 V			
..						
Ain_0	ai	Analog input to channel 0				
Sc_ext0-5	di	External slow control override. 6 pads. Pulled to DVSS via 10kohm resistor.	DVSS			
Sc_en	di	Enabling of the global slow control register. By default pulled to DVDD via 10kohm resistor. Connect to DVSS if the external SC pads are to be used.	DVDD			

Pad name	Type	Description	Nominal value	Typ. V (cur. Biases)	Max V. (mV)	Min V. (mV)
load	di	Load strobe for serial configuration register.	Logical			
regout	Do	Data output for serial slow control configuration register.	Logical			
regin	Di	Data input for serial slow control configuration register	Logical			
clkin	di	Clock for serial slow control configuration register.	Logical			
Sc_ext6-9	di	External slow control override. 4 pads. Pulled to DVSS via 10kohm resistor.	DVSS			
dvdd	p	digital vdd	+2.5 V			
avdd	p	Analogue vdd	+2.5 V			
avss	p	Analogue vss	-2.5 V			
dvss	p	digital vss	-2.5 V			
gnd	p	signal ground	0 V			
Sc_ext10-18		External slow control override. 9 pads. Pulled to DVSS via 10kohm resistor.	DVSS			
hold	di	used to hold analogue data, see fig.3	Logical			
dummy (holdb)	di	*)	Logical			
dreset	di	reset of digital part	Logical			
dummy (*dresetb*)	di	*)	Logical			
shift_in_b	di	start pulse for read-out	Logical			
dummy (*ck*)	di	*)	Logical			
ckb	di	clock for read-out register, see fig.3	Logical			
shift_out_b	do	Signalling end of read-out. Can be used as shift_in_b for next chip.	Logical			
Sc_ext19-20	di	External slow control override. 2 pads. Pulled to DVSS via 10kohm resistor.	DVSS			
Maresp	lvdi	Reset of the peak hold and TAC unit (not SC)	Low voltage differential			
Maresm	lvdi	Reset, negative phase.	Low voltage differential			
ta	do	ASIC trigger output (also used as sense line). Differential.	current mode logic			
tb	do	ASIC trigger output (also used as sense line). Differential.	current mode logic			

Pad name	Type	Description	Nominal value	Typ. V (cur. Biases)	Max V. (mV)	Min V. (mV)
Sc_ext21-22	di	External slow control override. 2 pads. Pulled to DVSS via 10kohm resistor.	DVSS			
vref	ai	Reference voltage for the differential analogue output buffer. Internally generated.				
Ibuf	ai	Bias-current for output-buffer. Int. generated.	220 µA 142 mV to AVSS			
ResWbi	ai	Bias-current for internal reset duration. Int. generated.				
Mo_vi	ai	Bias current for the trigger drivers. Int. generated.				
Shdelbi	ai	Bias current for the hold delay. Int. generated.	Int. gen			
Strbi2	ai	Bias current for peak hold device. Int. generated.				
Str_bi	ai	Bias current for peak hold device. Int. generated.				
Bufb2	ai	Bias current for slow shaper buffer. Int. generated.				
Mbias	ai	Master bias. All internal generated biases are derived from this reference.	700 µA -900mV			
Sha_b1	ai	Bias current for slow shaper. Int. generated.				
sha_bias	ai	Bias current for slow shaper. Internally generated.				
tbufbi	ai	Bias current for TAC output buffer. Int. generated.				
tbi	ai	Bias current for TAC. Int. generated.				
VTHR	ai	Threshold voltage for the discriminators.				
CGND	p	Reference voltage for the threshold	GND			
Trigwbi	ai	Bias current for width of the channel trigger pulse. Int. generated.				
obi	ai	Bias current for the discriminator. Internally generated.				
cvdd	p	Comparator vdd	+2.5 V			
cvss	p	Comparator vss	-2.5 V			

Pad name	Type	Description	Nominal value	Typ. V (cur. Biases)	Max V. (mV)	Min V. (mV)
vrc	ai	Control voltage to set the time constant in the HP filter before the discriminator. Internally generated.				
Vthrbi	ai	Bias current for the threshold alignment DAC. Int. generated.				
Bufb5	ai	Bias current for the fast shaper output buffer. Int. generated.				
Vfsf_clamp	ai	Bias current for fast shaper large signal clamp. Int. generated.				
vfsf	ai	Control voltage to feedback resistance in the fast shaper. Internally generated,				
Shaf_bias	ai	Bias current for fast shaper-amplifiers. Internally generated.				
Bufb4	ai	Bias current for the channel analog output buffer. Int. generated.				
avdd	p	Analogue vdd	+2.5 V			
avss	p	Analogue vss	-2.5 V			
Bleed	ai	Bias current for peak hold DC compensation. Int. generated.				
Outm2	ao	Negative output signal, TAC value (current)				
Outp2	ao	Positive output signal, TAC value (current)				
outm	ao	Negative output signal (current)				
Voutm	ao	Negative output signal (voltage)				
outp	ao	Positive output signal (current)				
Voutp	ao	Positive output signal (voltage)				
Bufb1	ai	Bias current for preamplifier output buffer. Int. generated.				

Pad name	Type	Description	Nominal value	Typ. V (cur. Biases)	Max V. (mV)	Min V. (mV)
pre_bias	ai	Bias current for pre-amplifiers. Internally generated.	700 µA -933 mV to AVSS			
vfp	ai	Control voltage to feedback resistance in pre-amplifier. Internally generated.	102 mV[1] to AVSS			
Dac_bi		Bias current for the preamplifier input voltage adjustment DAC. Int. generated.				
cal	ai	Calibration input signal				
Ain_63	ai	Analog input to channel 15				
..						
gnd	p	signal ground. 2 pads.	0 V			
avss	p	Analogue vss. 2 pads.	-2.5 V			
avdd	p	Analogue vdd. 2 pads.	+2.5 V			

Table 4: Description of pin and signal functionality.

- p = power, di = digital in, do = digital out,
- ai=analogue in, ao = analogue out,
- Logical = +2.5V (“1”) / -2.5V (“0”)

[1] see chapter ‘Useful Hints’

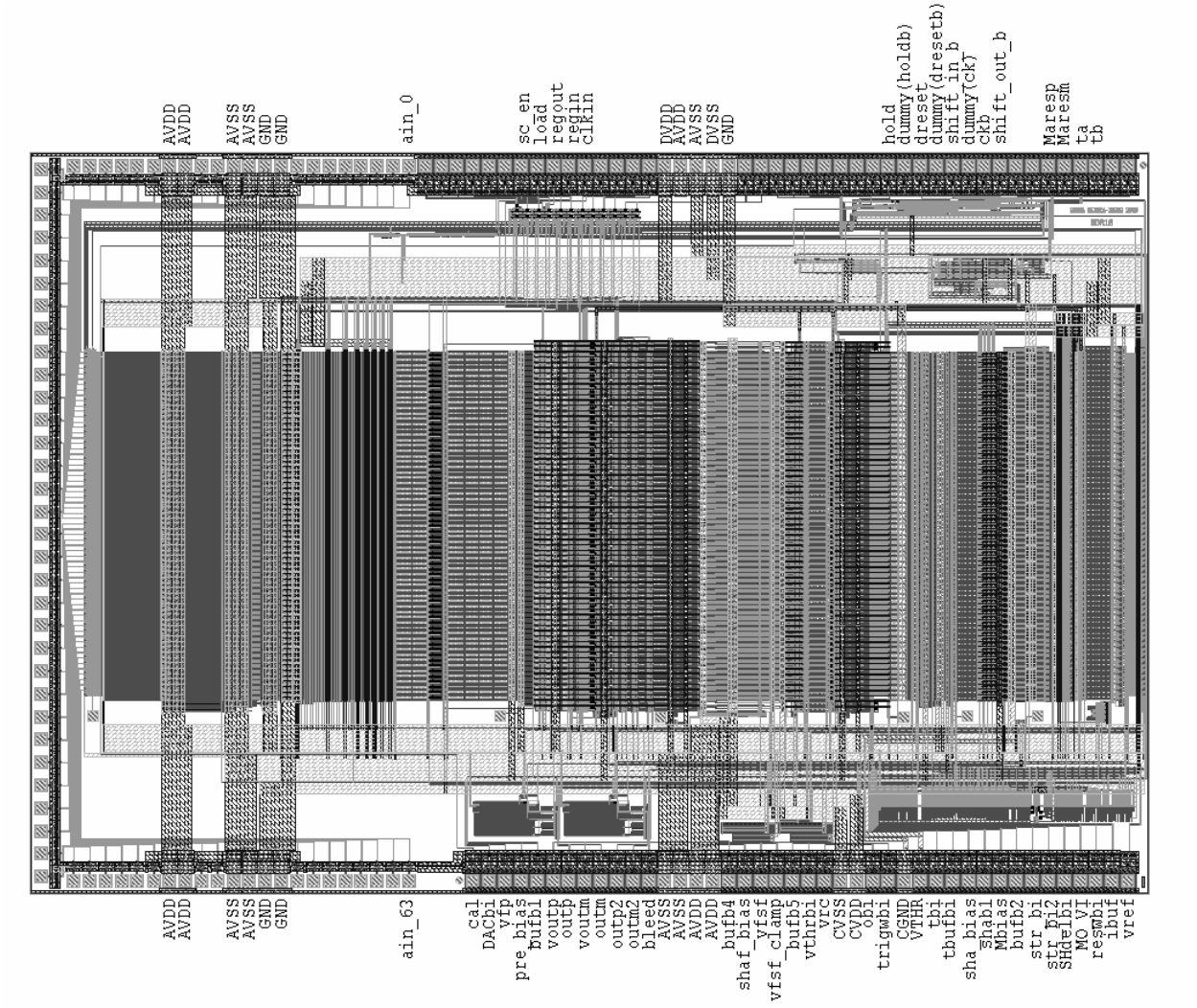

Figure 6: layout of the VaTA_HDR16. The die size is a total of 9.81mm * 6.5mm. All preamplifier input pads on the left side are located on a 200um pitch, the rest on the top and bottom side in a "horse shoe" structure. The input pads on the top and bottom sides are located on 140um pitch.