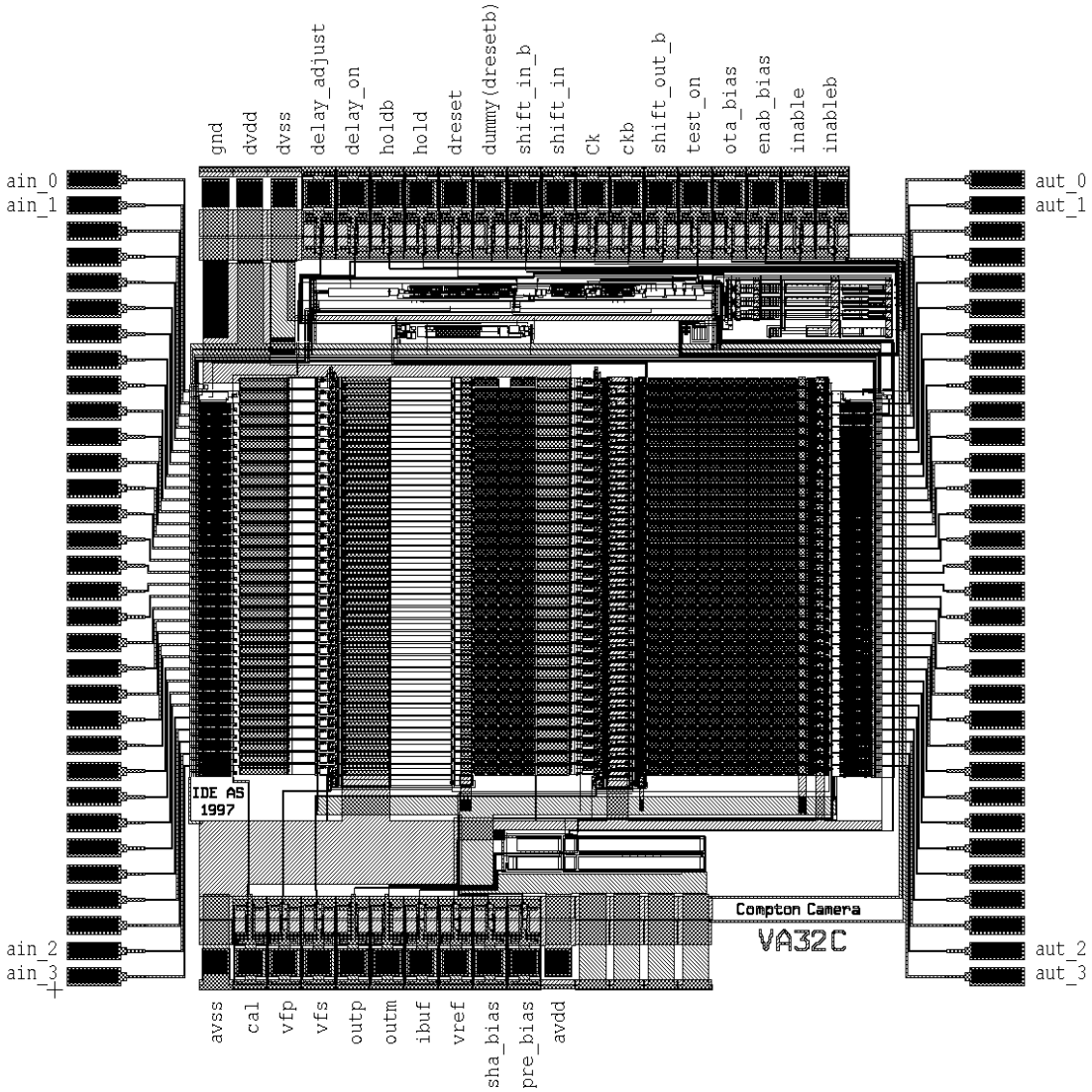
VA32C©

(TA - compatible)

Specifications



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1. General

÷ Description:

32-channel low-noise/low power high dynamic range charge sensitive preamplifier-shaper circuit, with simultaneous sample and hold, multiplexed analogue readout and calibration facilities. This circuit offers also a full parallel readout of all 32 channels.

÷ Vendor:

Integrated Detector & Electronics AS (IDE AS),
Veritasveien 9, N-1322 Høvik, Norway.

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÷ Availability:

Available as unpackaged, wafer tested dices or mounted on hybrids (dedicated or standard designs). Normally stock goods.

2. Physical

÷ Process:	1.2 µm N-well CMOS, double-poly, double metal.	
÷ Die size:	4067 µm x 3356 µm (including scribe) Thickness: ~ 600 µm	
÷ Input/ Output bonding pads:	Single row. Pad size: Pad pitch:	 50 µm x 200 µm 100 µm (see. fig. 2)
÷ Output, control and power pads:	Single row. Pad size: Pad pitch:	 90 µm x 90 µm 140 µm (see fig. 2)

3. Electrical

Power rails:	Vdd:	+2	V
	Vss:	-2	V

Each with separate connections for analogue (avdd and avss) and digital sections (dvdd, dvss) of the chip.

Back contact: metalized, connect to avss (-2V)

Current draw: Quiescent (typical values):

dvdd:	< 10	µA
dvss:	< 10	µA
avdd:	10	mA
avss:	-40	mA
gnd:	30	mA

Input bias currents: **(all driven to devices (e.g. resistors) referred to avdd)**

	Nominal			**Minimal values**[1]		
	pre_bias:	1000	µA	pre_bias:	100	µA
	sha_bias:	22	µA	sha_bias:	5	µA
	ibuf[2]:	140	µA	ibuf:	40	µA
Peaking time:	Nominal:	1.5	µs	Adjustable:	1	µs to 3 µs

Power dissipation:

Typical values:	Quiescent:	82	mW	Minimal:	11	mW

[1] With these settings, the performance may deviate from nominal specifications
[2] Only during readout

ESD Protection:	Inputs:	None
	Analogue out p & m:	None
	Controls (include. shift_out):	
	~ 300 Ξ series resistor and protection diodes to Vdd and Vss.	
Input stage:	Input device: PMOS referenced to gnd	
	Signal input potential: ~ -1.3 V to -1.4 V	
Gain:	~ 60 mV/fC nominal with differential outputs each driving 500 Ξ. Current gain is about 50 µA/fC. The gain depends on setting parameters like VFS, shaper bias etc.	
Linear range:	″ 2 MIP (can handle both signal polarities) 4 MIP in single polarity can be used with adjustment of VREF	
Noise (ENC):	Typical values:	
	40 + 12/pF e^- rms. for 2 µsec peaking time	
Readout:	Controlled via 32-bit (output) shift register.	
	Analogue outputs (outp, outm) of two or more chips can be connected in parallel to drive the inputs of an external, differential, transimpedance amplifier. Max. read-out is 10 MHz, here care has to be taken not to load the output buffer with to high capacitance and resistance.	
Calibration/test:	Voltage step applied via external 1.8 pF capacitor to the cal-input. 2 mV step represents 1 MIP (=22400e^- or 3.6 fC). Some additional noise has to be taken into account in test mode.	
	Calibration signal can be given to one channel in a given chip at a time. The channel is selected via a 128-bit (input) shift register.	

4. Pad Description

The output, control and power pads are listed below (see chip plot on next page, Figure 1.)

Pad name	Type	Description	Nominal value
gnd	p	signal ground	0 V
dvdd	p	digital Vdd	+2 V
dvss	p	digital Vss	-2 V
delay_adjust	ai	not in use	connect to gnd
delay_on	di	not in use	connect to dvss
holdb**)	di	used to hold analogue data, see fig.3	Logical
hold**)	di	*)	Logical
dreset	di	reset of digital part	Logical
dresetb	di	*)	Logical
shift_in_b**)	di	start pulse for read-out	Logical
shift_in**)	di	*) Connected to ground when not in use	Logical
ck**)	di	*)	Logical
ckb**)	di	clock for read-out register, see fig.3	Logical
shift_out_b	do	Signalling end of read-out. Can be used as shift_in_b for next chip.	Logical
test_on	di	Turns chip into test-mode	Logical
ota_bias	ai	***)	40 µA Vdd (when n.u.)
enab_bias	ai	***)	Vdd (when n.u.)
inable	ai	***)	Vdd (when n.u.)
inableb	ai	***)	Vss (when n.u.)
avss	p	Analogue Vss (+ chip backplane)	-2 V
pre_bias	ai	Bias current for pre-amplifiers.	500 µA
sha_bias	ai	Bias current for shaper-amplifiers.	22 µA
vref	ai	not in use. (recommended connected to decoupling capacitor).	
ibuf	ai	Bias-current for output-buffer.	140 µA
outm	ao	Negative output signal (current)	
outp	ao	Positive output signal (current)	
vfs	ai	Control voltage to feedback resistance in shaper-amplifier	700mV
vfp	ai	Control voltage to feedback resistance in pre-amplifier	-0.2 V[1]
cal	ai	Test input signal	1 MIP
avdd	p	Analogue Vdd	+2 V

p = power, di = digital in, do = digital out, ai = analogue in, ao = analogue out

*) Pads which should be used to connect complementary signals to the effective ones in order to minimise clock-feedthrough. If not used they should be grounded.
**) On these inputs are comparators differentially controlled by the signal and its complementary. This allows utilisation of reduced voltage-levels down to ±50mV.
***) If this chip is used with the TA chip (another IDE product) there are some additional featured available. For more information about this don't hesitate contacting us.

[1] see chapter 'Useful Hints'

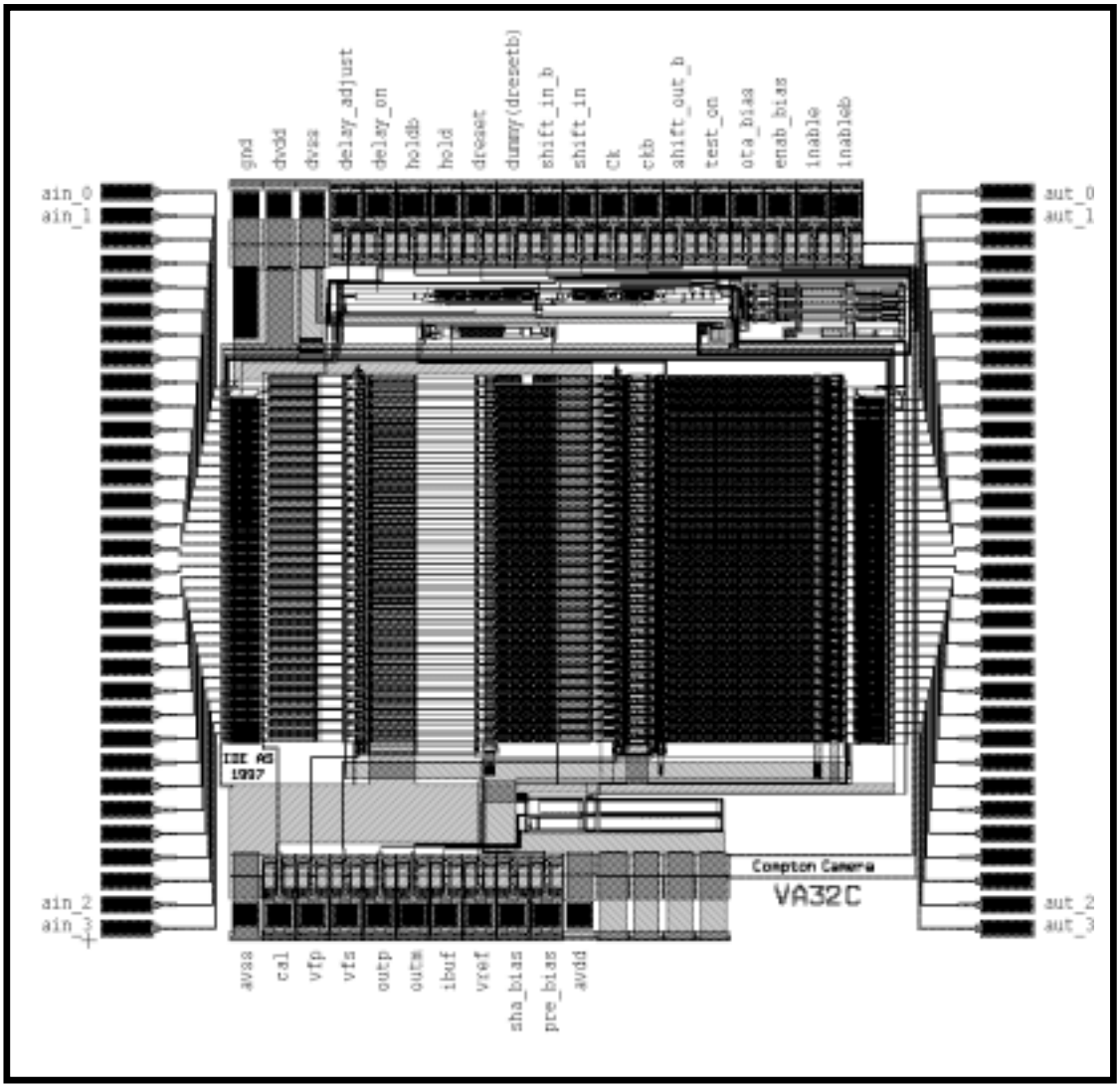

***Figure 1**. The VA32C chip with pad names.*

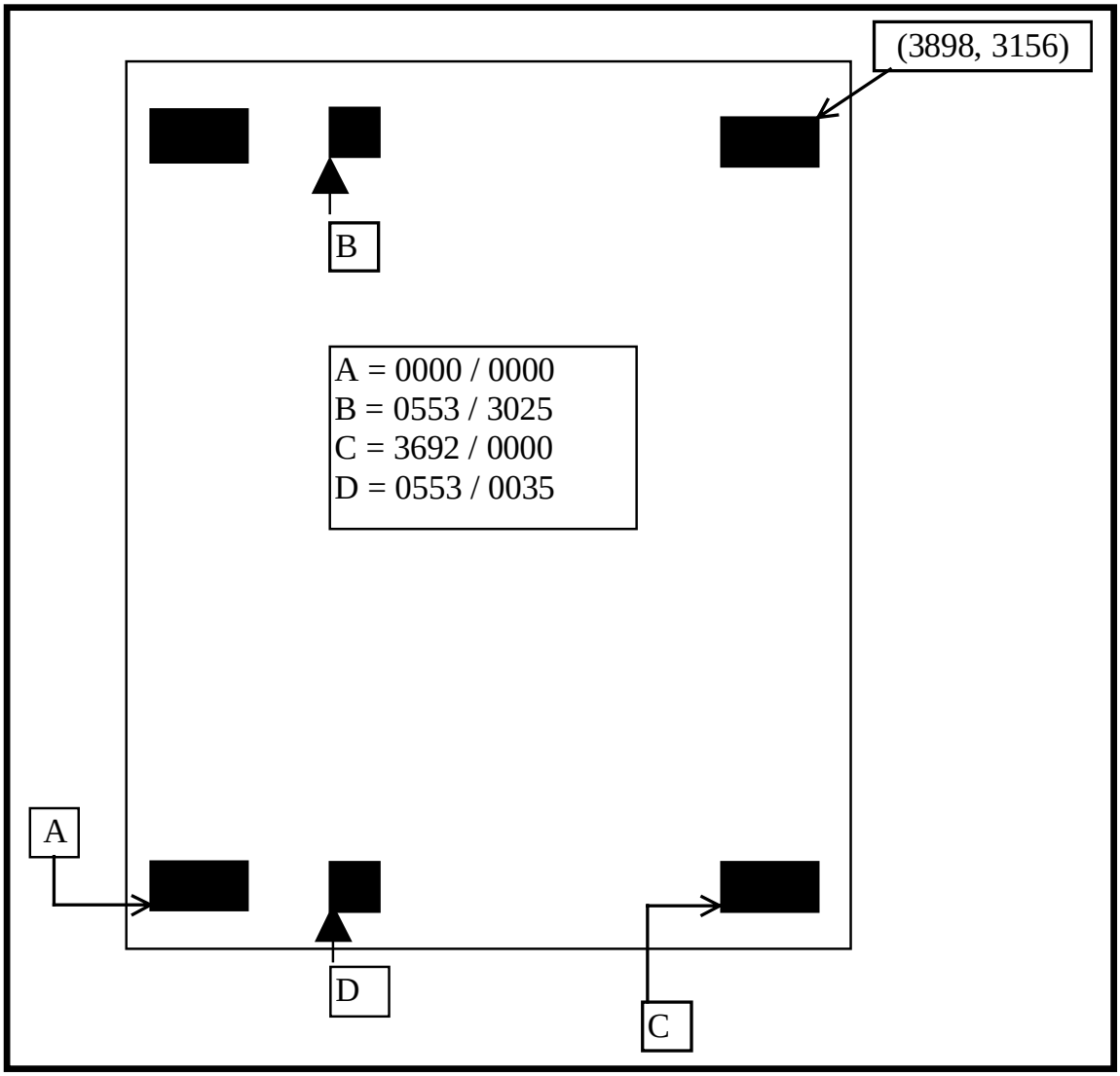

Figure 2. *Chip geometry & pad placement (Not to scale - all dimensions in µm). Please note that the referred co-ordinates are layout co-ordinates. Add 50 µm -100 µm on each side for scribe/cutting tolerances.*

5. Functional Description

As shown in Figure 3 the chip consists of 32 identical parallel charge sensitive amplifiers. The output of all amplifiers enters corresponding inputs of a 32-channel multiplexer. The switches in the multiplexer are controlled by a bit-register, which runs in parallel. The output of the mux. goes directly out of the chip via the output buffer (signal = '**outp**' - '**outm**'). Only one of the switches in the mux can be ¨on ¨ at a time. That is one amplifier (channel) at a time can be seen on the output of the chip. The bit in the register ripples in sequence from the top- to the bottom- channel by clocking '**ckb**'. The clock can be stopped at any point, which will leave the connection between the current channel, and the output, which remains enabled.

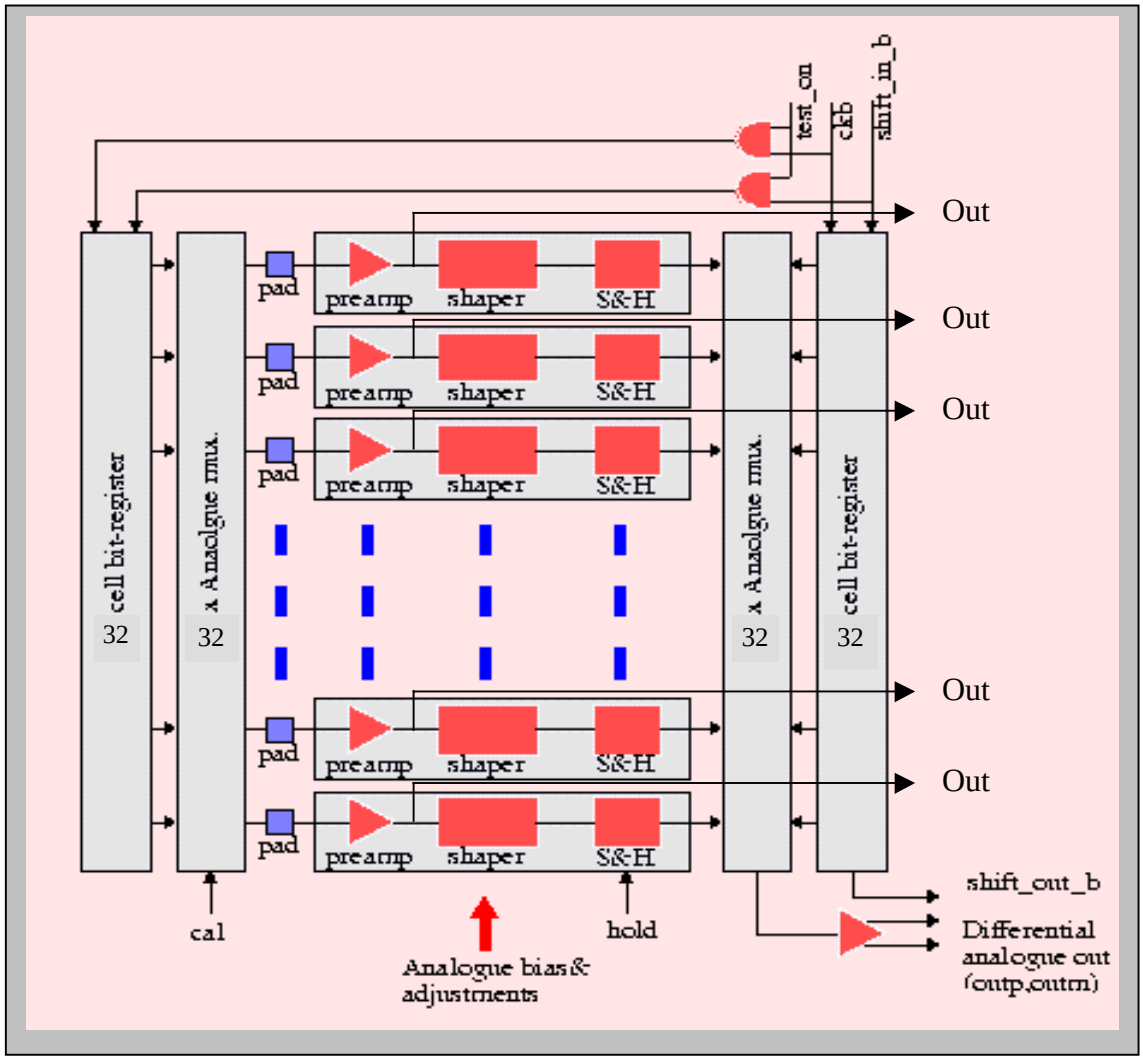

Figure 3. *VA32C Chip architecture and block diagram.*

6. Normal mode of operation

The normal mode of operation is that the 32 inputs are connected to a detector from where the charge signal comes. After the physics event, each channel will integrate its eventual signal for 500 ns. Usually, after the peak is reached (500 ns), an external '**holdb**' signal should be applied to sample the value. Immediately after this, a sequential read-out can be performed by activating the output bit-register using "**shift_in_b**" and "**ckb**". See Figure 4 for an example of the timing in this mode. The logic part of the chip can be reset either by applying the '**dreset**' or, simply by running through a normal read-out once.

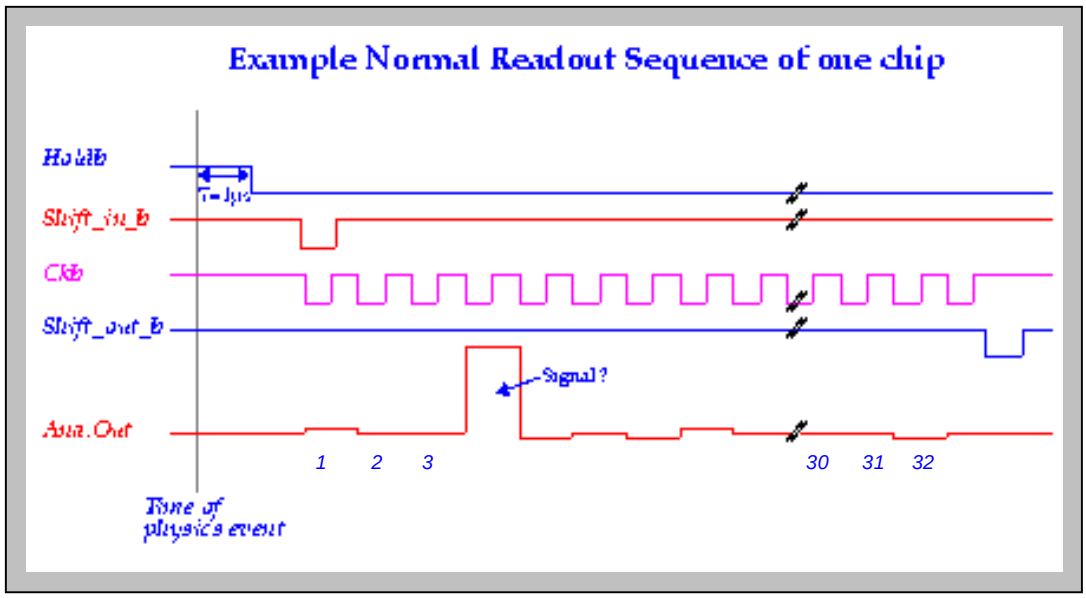

Figure 4. *Readout timing of the VA32C.*

7. Operation in test mode

Each of the inputs of the amplifiers can be accessed via the input pads on the left side, see Figure 4. In test mode, it is not necessary to connect any of these. Instead, the test facility of the chip can be turned on ('**test-on**'). This will enable another mux./bit-register on the input to run exactly in parallel with the output mux./bit-register. This input mux. connects all the inputs to the '**cal**' pad via a switch controlled by the bit-register. Also, in this case, only one connection at a time is possible and this connection will always correspond to the same channel as is connected in the output mux.

8. Useful hints

Use of 'cal'-input
When the '**cal**'-input is used in test mode an external capacitor (as close as possible to the pad) should be connected in series before the signal enters into the '**cal**' pad. A capacitor value of 1.8 pF is recommended. A voltage step of 20 mV gives hence an input signal charge of 36 fC (~10 MIP).

Generation of bias-currents/-voltages
Figure 5 shows a possible approach for generating the necessary bias currents and voltages.

Adjustment of VFP
VFP adjusts the feedback resistor of the pre-amplifier. Lower values result in a higher feedback resistor thus at too negative values the pre-amplifier will stop working.

Termination of outputs
Figure 6 shows a possible solution for termination of the outputs '**outm**' and '**outp**'.

Decoupling of power and bias lines

It is recommended to decouple the power and bias lines to GND.

9. Bias current generation

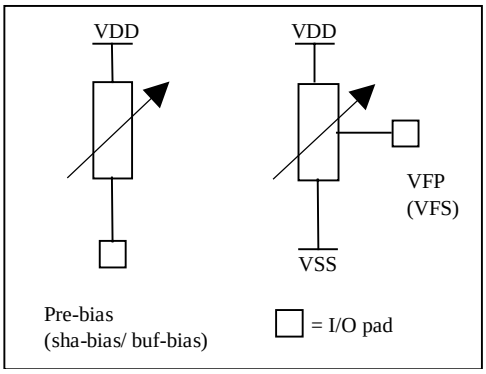

Figure 5. *Bias current and voltage generation*

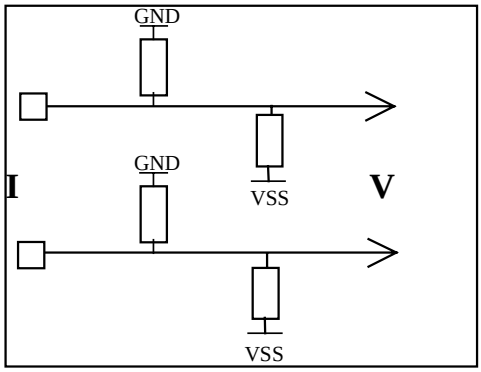

Figure 6. *Analogue "out" termination (1 kΞ recommended).*

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