Meeting minutes Compton PET ASIC meeting 19th April, 2007

Location: Gamma Medica-Ideas, Oslo.
Present: Peter Weilhammer, Enrico Chesi, Carlos Lacasta, Koki Yoshioka, B. Sundal, S. Mikkelsen. Neal Clinthorne participated in the last half of the meeing over the phone.

Technical discussion

Specifications for the new ASIC

- Application: Compton PET based on silicon detectors and scintillator, with several detector planes (10-12) in order to catch all events.
- Detector:
  - Small silicon pad detector, 1mm thick.
  - Leakage current: <100pA
  - Detector capacitance: 5-6pF
  - 1KeV=277 electron hole pairs
- ASIC specifications:
  - The design should be based on VATAGP3
  - If possible, make the new pad frame compatible with VATAGP3.
  - VATA-architecture
  - Slow shaper: 500ns. Values between 200-500ns were discussed, but the rate is low enough to allow for 500ns. This needs to be discussed in much more detail. Below 200ns, the ratio between the two shapers becomes small.
  - Fast shaper: 40-50ns. Optimized for good timing.
  - Charge polarity: Positive charges, or both positive and negative?
  - Linear range: 0-350KeV => ->15fC. The ASIC should have a good linear range up to 15fC, and a reasonable linearity up to 25-30fC.
  - Energy resolution: ideally 2-3KeV FWHM. This should be compared with the scintillator resolution, which is around 10-12%. 200e RMS would be a good number for the slow shaper.
  - Timing: for coarse coincidence timing, standard CR-RC shaping is the best solution. However, it is important that the signal is significantly higher than the threshold. The smallest interesting signal is 100KeV, and the threshold should be at least a factor 2.5 below this. We will aim for a factor 5. This will give us a timing resolution of 6-7ns FWHM.
  - The slew rate limitation of the fast shaper can be turned on with the configuration shift register.
  - Threshold: design goal is 15-20KeV = 4100-5550e.
  - Calibration scheme: we can revisit the calibration scheme, but if new functionality is implemented, there should be a safe back-up solution. Please send proposals for a new structure if desirable.

Administrative discussion

- Need safe solution that can be used for demonstrator now. One more iteration can be foreseen later.
- Need the ASIC by the end of the year. To make this happen, GM-I needs to put the chip on the planned September run.
- Base cost for putting a design on a run in 0.35um technology is EURO60K. This includes prototype testing, test card design, test report and delivery of 100 ASICs.
- It is OK to get 120 ASICs for this price.
- Need a decision quite soon if we want the slot on the Sept. run.

Action items

- GM-I will check if it is possible to extend the linear range up to 40-50fC.
- Peter will send detector data that can be used in simulation.
- Before a design phase is started, we should set up a phone conference or another meeting in Oslo to go carefully over all experience related to ASIC instability and perform a final Design Review.

Feedback on previous ASICs GP3.1 and GP5

Neal pointed out that pedestal change has been seen when using the ASIC in different RO modes. This is related to pick-up, either on the hybrid or the ASIC. Peter: this is related to the hybrid design.

In addition, most of the issues with the previous ASICs were summarized in Enrico's document, see below. Our comments are inserted into the text with bold letters:

Résumé of measurements on VATA chips

Up to now, three chips have been used and tested, namely the GP3, GP3_1 and the GP5. The GP3 has been extensively used in the Compton Camera project, the GP5 in the brain PET and the GP3_1 was mainly tested in the laboratory.

The following is a reminder of known drawbacks of each integrated circuit.

GP3

The GP3 basically works well. It has been widely used for the Compton Camera project. An extensive series of measurements have been performed (for what we are concerned, see the report from Peter and myself).

The GP3 has a programmable amplifier in the fast branch, in order to change the range of the discriminators. There are 4 possible programmable gains (from 0 to 3). If the chosen gain is 0, for a positive input charge the discriminators threshold voltage must be negative, while for all the other gains the threshold voltage must be positive (there is a polarity inversion in the amplifier).
If you choose a gain other than 0, the chip oscillates!

1. **GM-I: We should make an effort to analyze all experience seen with all three previous ASICs, and take it into account in the new design. This will be one of the main focuses for the new design. Since the last version of these ASICs, we have accumulated design experience that we believe will be very useful for handling this issue.**

GP3-1

GP3_1 should have the same performances as the GP3, with a difference in the fast branch. There in fact a time-walk compensation for the generation of the output triggers.

Another difference respect to the GP3 is the absence of the programmable amplifier in the fast branch, therefore the threshold voltage must be positive for a positive input charge. As a consequence, we had many problems with oscillations and instabilities.

2. **GM-I: See item 1**.

Another drawback is the malfunctioning of the read-out in sparse mode. In fact, it is possible to read one chip alone, but when you have 2 chips daisy chained, you can read data only from the second one, the first is skipped. One way to make it work is to use the read-out in sparse + adjacent!!!!!!

3. **GM-I: This circuitry has been process migrated, improved and tested and should now be working.**

The GP3_1 is very unstable and sensitive to the hybrid on which is mounted. We had problems going from a hybrid with a thickness of 1.2 mm to one that was only 0.6 mm, for reasons that are not known.

4. **GM-I: See item 1-2, it is likely that there is a connection between these observations**.

GP5

The GP5 is a chip with a high dynamic range (~ 1 pC) and therefore the levels of the signals and the threshold voltage of the discriminators are much higher than the ones in the GP3 and GP3_1.

The peaking time of the signals in the slow and fast branch, are respectively 300 and 50 nS, compared to the 4uS and 150 nS of the GP3 and GP3_1.

The GP5, as the two other chips, does not have the programmable amplifier in the fast branch. It works with a positive threshold voltage for input positive input charges. It does not oscillate.

When operated with supply voltages at the nominal values, it shows a strong non linearity on the slow branch. In order to make it work correctly, the supply voltages must be -2.3V and +2.2V respectively.

5. **GM-I: The cause of this is not known, but we will take care in a new design to achieve good linearity for the desired DNR.**

The GP5 shows also the problem of the sparse read-out: if you have 2 chip daisy chained, it is possible to read the data from the second chip but not from the first one. To avoid this problem, the trick is to use a MBias 30% lower than the nominal (this had no effect on the GP3_1).

6. **GM-I: See item 3, we assume that the effects are related.**

The GP5, as the GP3_1, has a time-walk compensation circuit. Measurements have shown that for signal larger than ~ 20 KeV, the time-walk is smaller if the time walk compensation is switched off. With the time compensation off, the response of the fast branch is a pure CR – RC, and for charges between 30 KeV and 1 pC, the time-walk is in the order of 5-7 nS.

7. **GM-I: We will by default turn off the time walk compensation, and include a configuration bit to turn the feature on.**

Cosiderations about the new chip

The new chip must probably be between the GP3 and the GP5. Here is a list of possible desiderata or suggestions for the new chip. Of course, everybody can join and give his own contribution. The list is made with no logical order.
From now on, for sake oh shortness, the new chip will be referred to as the “Baby”!

8. As the GP3 seems until now to be the best circuit, I would suggest that Baby should follow as much as possible the GP3. Of course the peaking times of the fast and slow branch must be modified according to the needs.
    - **GM-I: OK, this will be taken into account. However, we have during the last 3-4 years done a lot of development that also will be used in this project, like previously process migrated components.**

9. Can Baby have the same foot print as the GP3? This would help enormously with the existing hybrid for testing.
    - **GM-I: We will try to make the pad frame as similar as possible, if no technical issues are found.**

10. All the existing chips have the pads DL and DLb only on the right side. This is annoying if the chips are mounted very close together, as is difficult to have two common lines running across in that region. We suggest that Baby will have these pads on both side of the chip, so that they can be daisy-chained from chip to chip
    - **GM-I: This is OK.**

11. We have shown that with the trim DAC's is possible to make the thresholds of the channels more uniform. The GP3 has 3 bits, giving 4 positive and 4 negative values. Each bit has a weight of about 1-2 mV. The weight is O.K. but the number of bits should be increased (4 bits ?). This would allow compensation not only between channels of the same chip but also between different chips. An even better solution would be to have trim DAC's on each channel of the chip (4 bits, weight 1-2 mV) and a DAC acting on the common threshold of each single chip. This would allow first a compensation of the channels of each single chip and the calculation of the average thresholds and then the second DAC would then be used to equalize the averages of the different chips.
    - **GM-I: All new ASICs have 4 bit per channel for threshold trimming. These DAQs are of the sink-source type, that ideally removes all return current from the threshold line. In addition, it is standard to have a 5-6 bit global DAC for adjusting the threshold between ASICs.**

12. When using DAC compensation, if the number of positive bits is different from the number of negative bits, a current flows on the common threshold line. This does not matter if the source of the threshold voltage is a low impedance device capable of sourcing / sinking current. Unfortunately, very often we mount in series with the threshold generator a resistance (~ 1k) in order to avoid hysteresis. If oscillation starts at a threshold value of, let's say, 20 mV, to kill the oscillations we must raise the threshold to 30 mV or above. Working between these two limits is dangerous. When the system oscillates, a current is generated on the common threshold line. If a resistance is present on the threshold line, this current automatically increases the threshold voltage stopping the oscillations. The hysteresis disappears. But if we have a resistance on the threshold line, the compensation with the trim DAC's is not possible. Can we avoid generating a current on the threshold line when using the trim DAC's?
    - **GM-I: See above**.

13. Can Baby have a more friendly way of injecting a calibration pulse? The best would probably to have an internal voltage divider so that we can supply from externally a decent (in size) pulse, that will be divided internally to the required value.

- **GM-I: TBD. Internal voltage divider could be risky due to pick-up from return currents etc. We are open for discussion, but if we should implement a new scheme, we will implement a by-pass switch such that we can use the old scheme.**

14. Baby should not implement the time-walk compensation circuit but use instead a normal CR-RC circuit on the fast shaper. From measurements done on the GP5, we have seen that if in the proper charge range, the time-walk is smaller if the compensation circuit is not active.
    - **GM-I: By default, time-walk compensation will be off. However, it can be turned on by setting a bit in the configuration register.**

This is for the moment what I can think of for a new integrated circuit. Everybody is invited to join with suggestions. Thank you!

Geneva, 15/04/07 E. Chesi