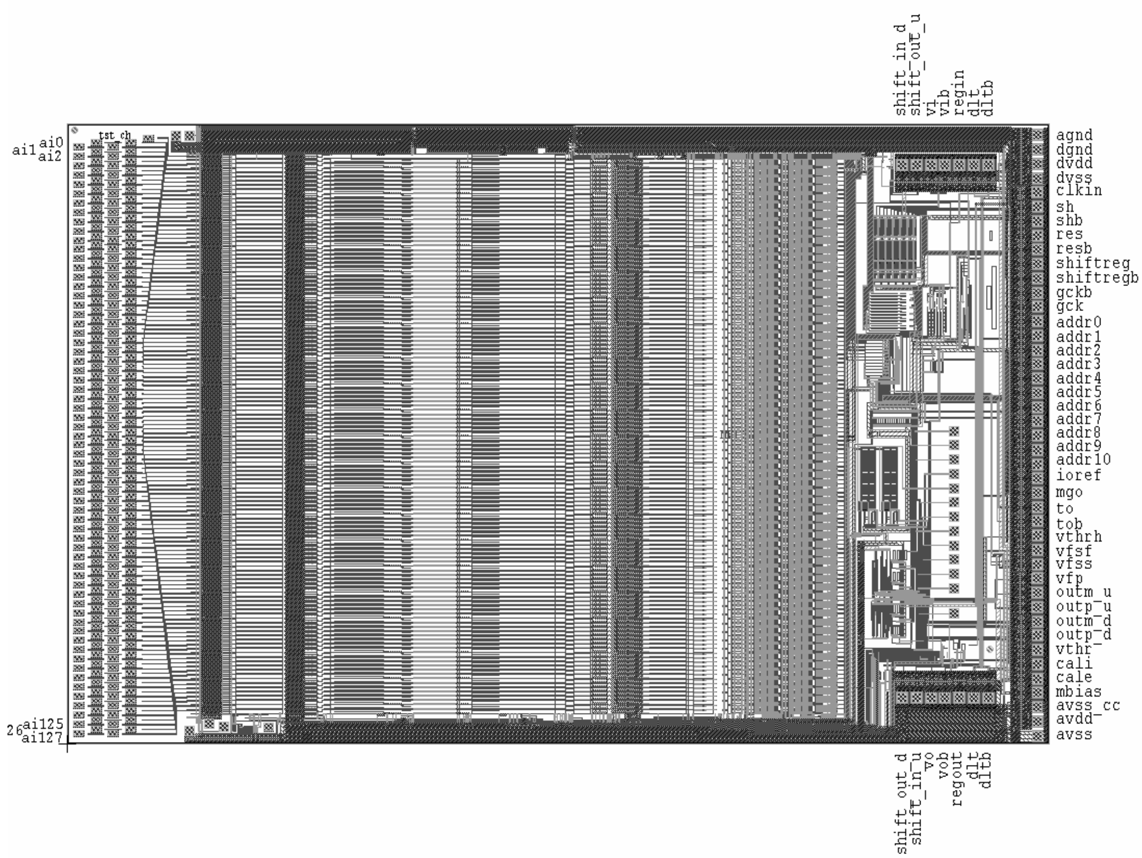
VATAGP7



V0R3

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1 General

The VATAGP7 is a 128-channel "general purpose" charge sensitive amplifier, based on the VATAGP3. It is pad compatible with VATAGP3. Each channel features low-noise/low-power buffered preamplifiers, a shaper with sample/hold, multiplexed analogue readout and calibration facilities. In addition, each channel has a fast shaper that gives a trigger signal. The analogue value and the address of the triggering channels are read out with a flexible serial or sparse read-out system. The VATAGP7 also offers input leakage current compensation automatically adjusted in each preamplifier channel.

The ASIC is equipped with a test channel for probing the fast shaper output.

The TA-part includes a 4-bit threshold trim DAC for each channel and a 5 bit global threshold trim DAC.

The VATAGP7 is designed for use in systems employing many chips in parallel, sharing some control lines and all output lines with the other modules.

1.1 Changes from VATAGP3

The main changes from the VATAGP3 are as follows:

1. Gain and peaking times for the slow and fast shapers.
    a. There is no gain-stage.
    b. Fast shaper peaks at 50ns (nominal)
    c. Slow shaper peaks at 500ns (nominal).
    d. Both positive and negative polarity.
2. 4 bit "sink-source" threshold trim DACs per channel
3. New calibration circuitry accepting a digital input signal. The amplitude of the internally generated cal pulse is set by a DAC.
4. DLT/DLTb pads available on the top and bottom side of the ASIC for daisy chaining.
5. Possibility to turn on/off the fast shaper slew rate compensation with the slow control.

2 General functionality

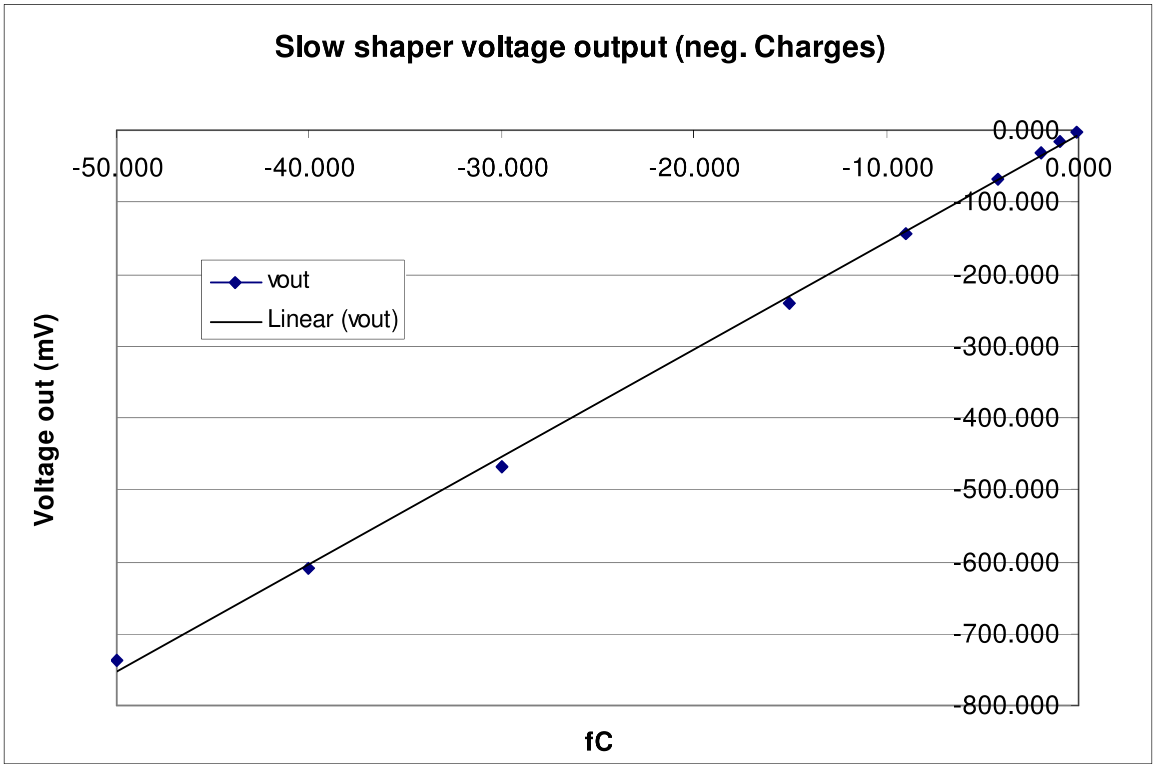
2.1 General

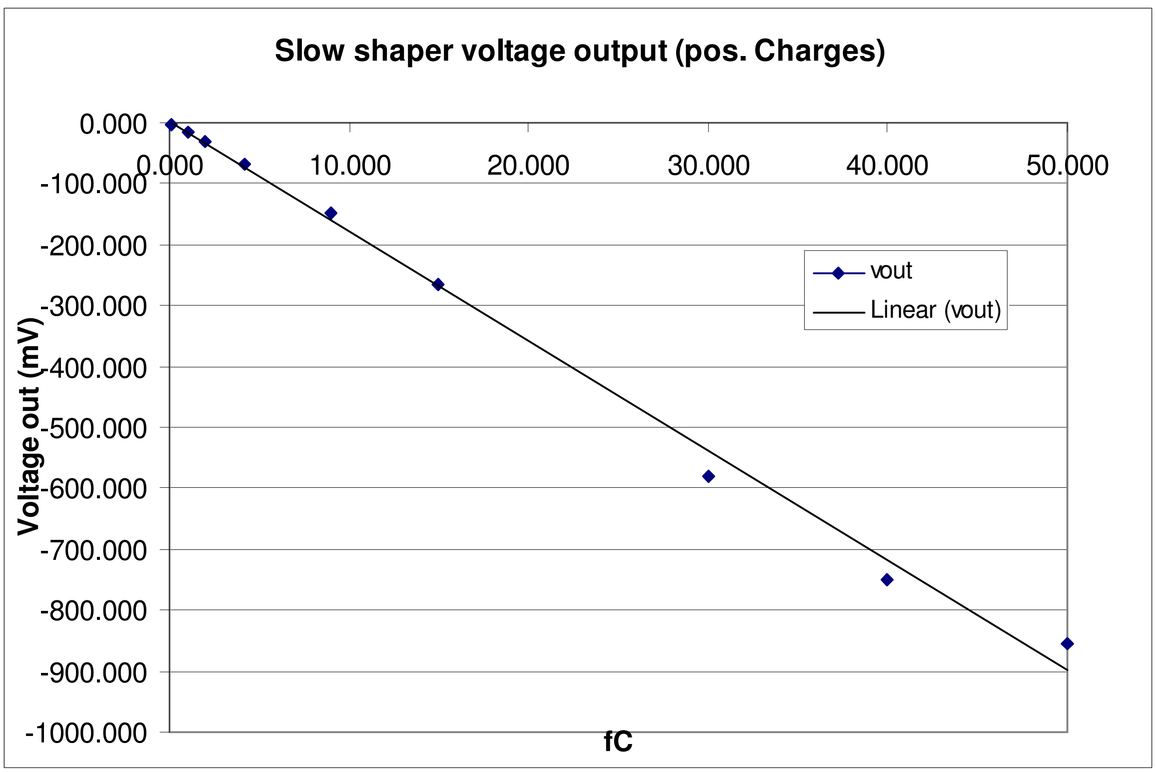
Parameter	Conditions	Value	Units	Comment
Number of channels		128		

2.2 Analog Specifications

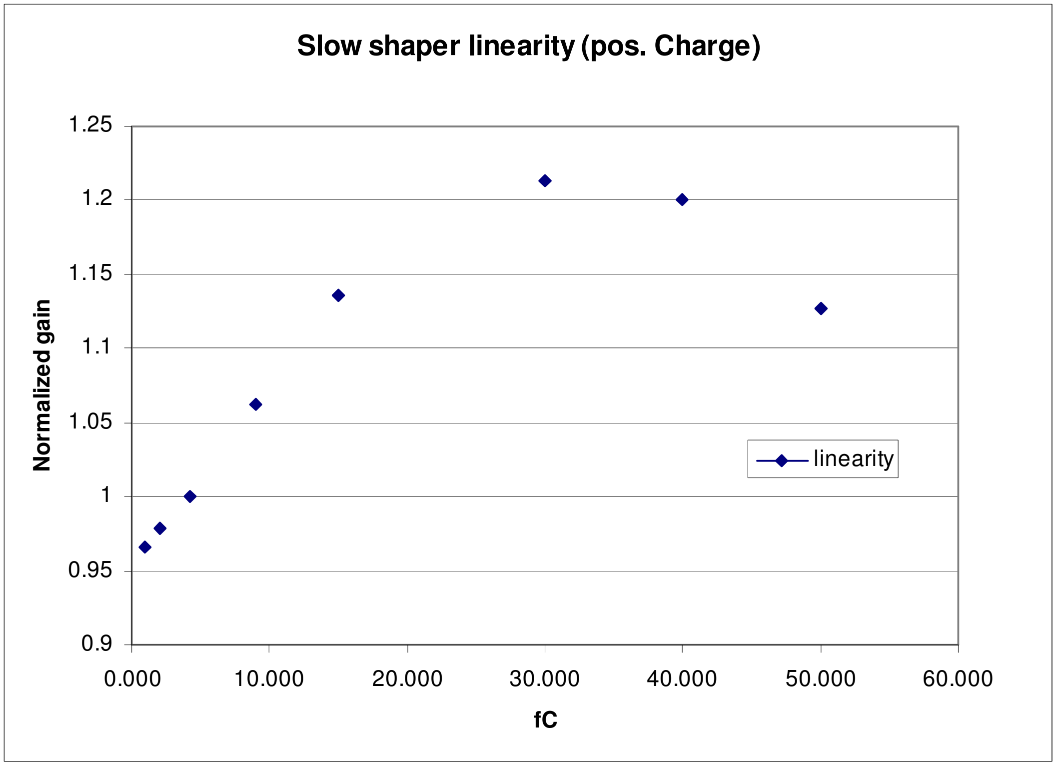
The values given in this section are typical figures based on simulations. All parameters are simulated at room temperature, with default biases and voltage supply levels.

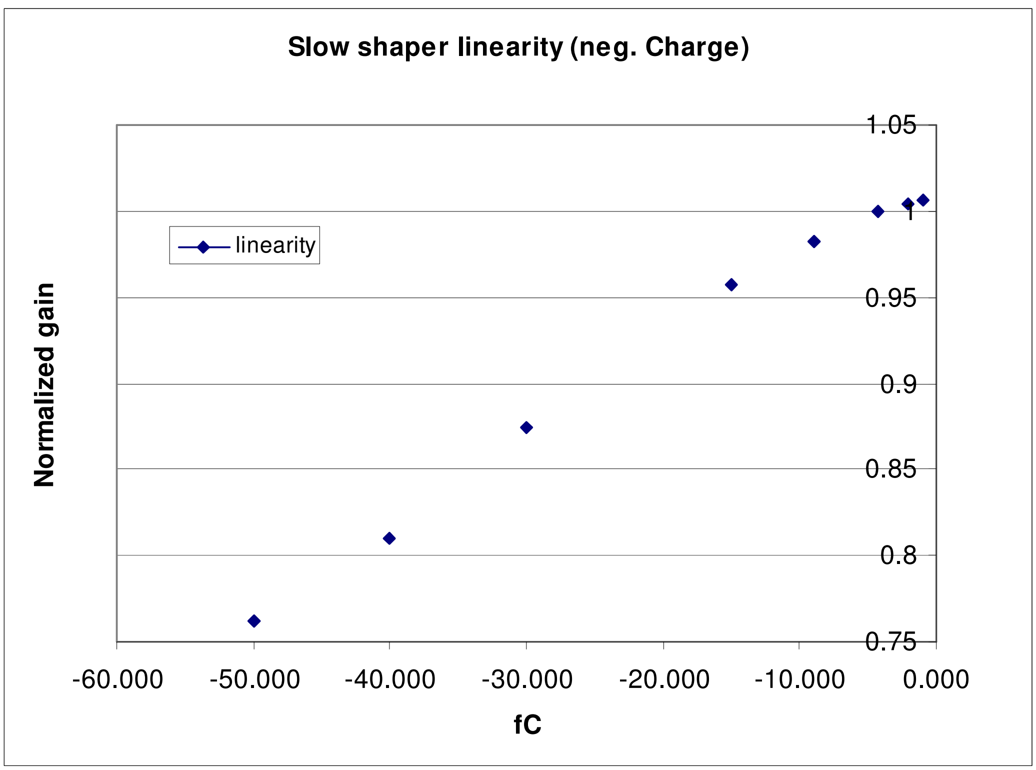
Parameter	Conditions	Value	Units	Comment
Gain	From input to output of output buffer	16.5	µA /fC (typ)	The differential output currents are summed
Input potential of preamplifiers	Referenced to AGND	-1.0 to -1.2	V (typ)	
Electronic (thermal) noise	Zero input capacitance, zero leakage current	70	e^- (typ)	Default biases
Electronic (thermal) noise, slope		12	e^-/pF (typ)	
Leakage current noise, slope			e^-/nA (typ)	Note: noise contributions add in quadrate
Dynamic range		+/-30	fC (typ)	The nominal range is up to 30fC but the asic will not saturate until 50 fC. Good linearity up to +/-15 fC.
Lowest threshold	No input capacitance	0.12	fC (typ)	No load, 5 sigma from noise floor.
Lowest threshold	6pF load	0.3	fC	6pF load at preamp input., 5 sigma from noise floor.
Peaking time (Slow shaper)		400 500 900	ns (min) ns (typ) ns (max)	Adjustable by overriding of biases. Default Adjustable by overriding of biases
Peaking time (Fast shaper)			ns (min)	Adjustable by overriding of biases
		50	ns (typ)	Default
			ns (max)	Adjustable by overriding of biases





Simulated linearity for positive and negative charges for the slow-shaper. The shaper is optimized for charges up to +/- 15 fC.





Nonlinearity for the slow shaper, for positive and negative charges.

2.3 Mechanical and Process

The figures given for the Human Body Model are typical values, but have not necessarily been measured for all pins.

Parameter	Conditions	Value	Units	Comment
Manufacturing process		0.35	µm	CMOS, NOT epitaxial layer wafers
Die size, length	Not including scribe.	9895	µm	From preamplifier inputs to parallel outputs
Die size, width	Not including scribe.	6120	µm	
Thickness		725	µm (typ)	
Bonding pad pitch	Double row Single row	91.2 140	µm µm	Preamplifier input pads Control, output, bias, and power pads
Bonding pad size	Double row	90 x 50 90 x 90	µm µm	Preamplifier input pads (and preamp output) Control, output, bias, and power pads
Bonding pad series resistance		0 0/300	Ω Ω	Preamplifier input pads and parallel output Control, output, bias, and power pads
Bonding pad ESD protection	Measured by the Human Body Model. Measured by the Human Body Model.	2000 >2000	V (typ) V (typ)	Preamplifier input pads, protection diodes. Control, output, bias, and power pads

3 Power supplies

Parameter	Value	Description, comment
Power supply: AVDD	+1.5V ref. AGND	Positive power supply for the preamplifier and shaper.
Power supply: AVSS	-2.0V ref. AGND	Negative power supply for the preamplifier and shaper. Connect to ASIC back plane.
Power supply: AGND	0V	Ground for the preamplifier. Note: the detector bias must be decoupled to this ground close to the ASIC.
Power supply: DVDD	+1.5V	Power for the digital back-end
Power supply: DVSS	-2.0V	Ground for the digital back-end
Back contact	-2.0V	Connect to AVSS
Current consumption, +1.5V supply, 128 channels	40mA	Current consumption from AVDD+DVDD. Current is into ASIC.
Current consumption, 0V supply, 128 channels	40mA	Current consumption from AGND. Current is into ASIC.
Current consumption, -2V supply, 128 channels	80mA	Sum of the two currents above. Current is out ASIC.

Parameter	Value	Description, comment
Power dissipation per channel	~2.2 mW	Approx.

4 Pad Description

Bias pads which do not require bonding (internally generated or pull-up/pull-down) can be bonded for external decoupling, adjustment or forcing. Pads described clock-wise from upper left to lower left (excluding input pads). Positive current direction is into the chip.

Pad-row on the ASIC top side:

Pad name	Type	Description	Nominal value
shift_in_d	di	Shift register input (downwards)	logical
shift_out_u	do	Shift register output (upwards)	logical
vi	ldi	Veto input (pos. phase)	low v. logical (pd)
vib	ldi	Veto input (neg. phase)	low v. logical (pu)
regin	di	Data input for control register	logical (pd)
dlt	di/do	Disable late trigger (pos. phase)	current
dltb	di/do	Disable late trigger (neg. phase)	current

Pad-row on the ASIC right side:

Pad name	Type	Description	Nominal value
AGND	p	Signal ground for the analogue part	0 V
DGND	p	Connect to AGND	0 V
DVDD	p	Digital vdd	1.5 V
DVSS	p	Digital vss	-2 V
clkin	di	Clock for control register	logical
sh	ldi	Sample and hold (pos. phase)	low v. logical
shb	ldi	Sample and hold (neg. phase)	low v. logical
res	ldi	Reset of the readout logic (pos. phase)	low v. logical (pd)
resb	ldi	Reset of the readout logic (neg. phase)	low v. logical (pu)
shiftreg	ldi	Readout mode (pos. phase)	low v. logical (pu)
shiftregb	ldi	Readout mode (neg. phase)	low v. logical (pd)
gckb	ldi	Clock for readout (neg. phase)	low v. logical
gck	ldi	Clock for readout (pos. phase)	low v. logical
addr0-6	do	Digital output of hit channel address	current

Pad name	Type	Description	Nominal value
:	:	:	:
addr7-10	do	Digital output of chip address	current
ioref	ai	Current sink for the address output buffer	Connect to ~0V
mgo	ao	Multi-hit trigger output	current
to	ldo	Trigger out (positive phase)	current
tob	ldo	Trigger out (negative phase)	current
vthrh	ai	High threshold for the discriminator	2V /-2V? (depending on signal polarity)
vfsf	ai	Control voltage for the feedback resistor (NMOS) in the fast shaper	-125 mV pos. sig. -300 mV neg sig. (int. gen.)
vfss	ai	Control voltage for the feedback resistor (NMOS) in the slow shaper	-150 mV pos. sig. -350 mV neg sig. (int. gen.)
vfp	ai	Control voltage for the feedback resistor (NMOS) in the preamplifier	-610 mV pos. sig. -550 mV neg sig. (int. gen.)
outm_u	ao	Diff. analog output, neg. phase (upwards shiftregister)	0-200 uA
outp_u	ao	Diff. analog output, pos. phase (upwards shiftregister)	0-200 uA
outm_d	ao	Diff. analog output, neg. phase (downwards shiftregister)	0-200 uA
outp_d	ao	Diff. analog output, pos. phase (downwards shiftregister)	0-200 uA
vthr	ai	Normal threshold for the discriminator	> 50 mV?
cali	ai	Test pulse with internal capacitor	voltage step
cale	ai	Test pulse with external capacitor	charge
mbias	ai	Bias reference for all the internally generated biases	500 uA
AVSS_CC	ai	Reference for current compensation	–2 V
AVDD	p	Analog vdd	1.5 V
AVSS	p	Analog vss	-2 V

Pad-row on the ASIC bottom side:

Pad name	Type	Description	Nominal value
dlt	di/do	Disable late trigger (pos. phase)	current
dltb	di/do	Disable late trigger (neg. phase)	current
regout	do	Data output of the control register	logical
vob	ldo	Veto output (neg. phase)	low v. logical
vo	ldo	Veto output (pos. phase)	low v. logical
shift_in_u	di	Shiftregister input (upwards)	logical

Pad name	Type	Description	Nominal value
shift_out_d	do	Shiftregister output (downwards)	logical

p = power, di = digital in, do = digital out, ldi= low voltage differential digital in,
ldo= low voltage differential digital out, ai=analogue in, ao = analogue out,
pu = pull-up, pd = pull-down
Low voltage logical = 0V("1") / -0.2V("0")
Logical = +1.5V ("1") / -2V ("0")

Pads on the second pad-row, listed from upper to lower. These pads are for over-riding of internally generated biases.

Pad name	Type	Description	Nominal value
vrcp	ai	Control voltage for HP -filter resistor (PMOS) in front of discriminator	-560 mV neg. sig. (int. gen.)
vpz	ai	Control voltage to feedback resistance in gain stage.	
Obi_indrv	ai	Bias for the input receivers	90 uA (int. gen.)
Mo_bi	ai	Bias for the address and mgo current sources.	-140 uA(int.gen.)
vref	ao/ai	Reference for the output buffer, internally generated by a dummy slow shaper	~500 mV
twb	ai	Trigger width bias	-10 uA (int. gen.)
sbif	ai	Bias for the fast shaper	22 uA (int. gen.)
vrcn	ai	Control voltage for HP -filter resistor (NMOS) in front of discriminator	790 mV pos. sig. -2V neg. sig. (int. gen.)
prebias	ai	Bias for the preamplifiers	500 uA (int. gen.)
sbis	ai	Bias for the slow shaper	22 uA (int. gen.)
ibuf	ai	Bias for the analog output buffer	225 uA (int. gen.)
ref_bi	ai	Bias for threshold DACs	10 uA (int. gen.)
obi	ai	Bias for the discriminators	90 uA (int. gen.)

5 Layout

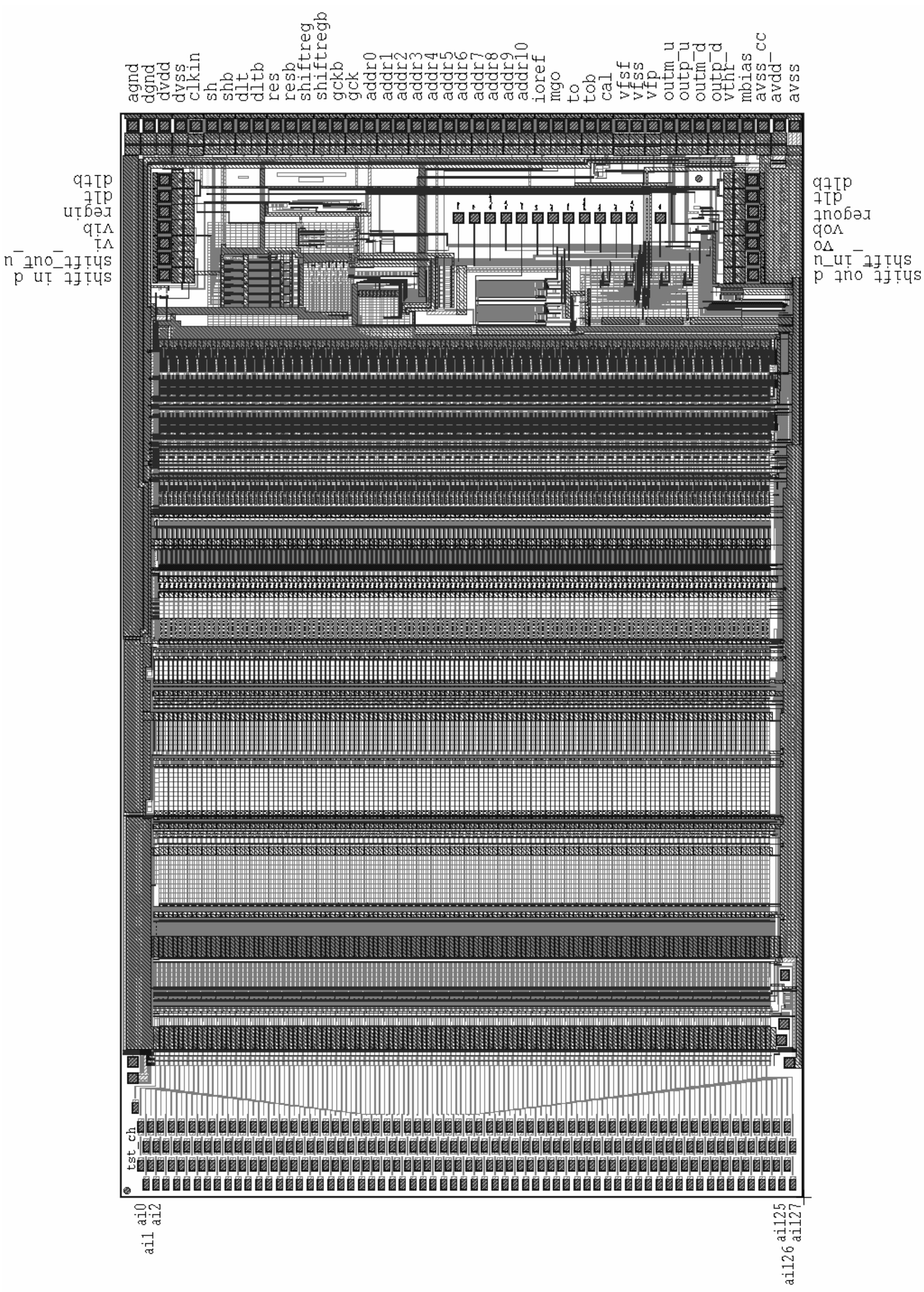


Figure 1: Preliminary chip plot of the VATAGP7.

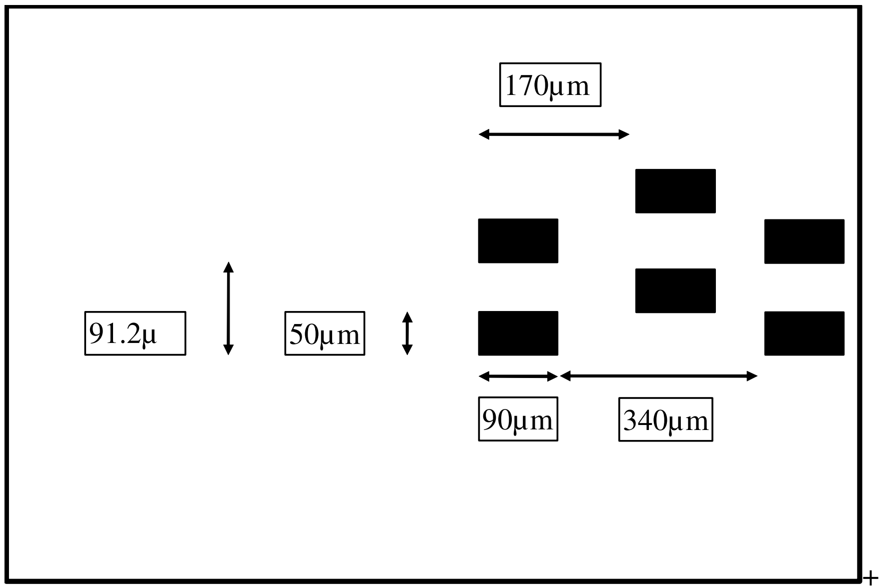
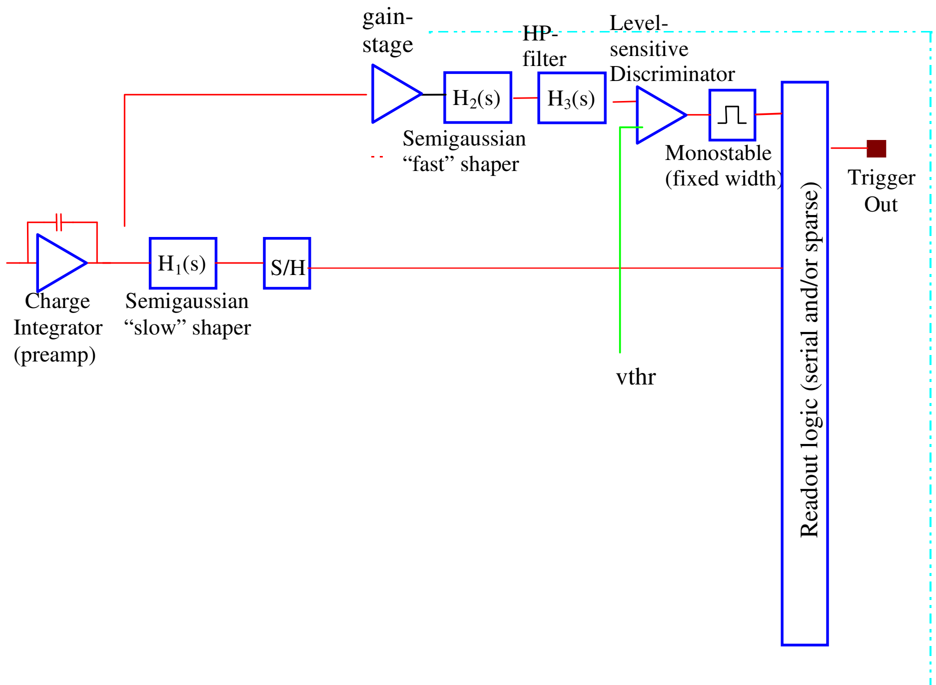


Figure 2: Definition of input pad size and pitch.

6 Functional description:



(See the following text for more detailed information)

6.1 Using VATAGP7 in parallel:

The VATAGP7 is designed to be used in parallel for reading out a large number of channels. There are 4 bits for the chip address, giving a maximum of 16 chips on the same bus, with a total of 2048 channels. The pads are placed such that signals going from one chip to the next are on the opposite side. This makes the PCB routing easy. The signals should be connected as shown below: (chip number in parenthesis)

vo(1) to vi(2)
vob(1) to vib(2)
shift_out_u(1) to shift_in_u(0)
shift_out_d(1) to shift_in_d(2)
regout(1) to regin(2)
inp_drain(1) to inp_drain(2)

All other control signals should be in parallel.

6.2 Biasing

The VATAGP7 is designed to have only one external bias: *mbias*. All other biases are internally generated, where all biases are a fraction of *mbias*. However, sometimes it is necessary to adjust or force the biases to other values than the nominal. Pads are available for all biases making external adjustment is possible.

Generation of bias currents/voltages

Figure 3 shows a possible approach for generating the necessary bias currents and voltages.

mbias is a current **into** the chip (resistor to VDD).

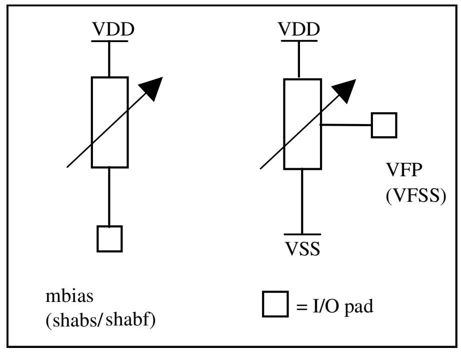


Figure 3: Bias current and voltage generation

Decoupling of power and bias lines

It is recommended to decouple the power and bias lines to GND.

Use 100 nF ceramic capacitors on the power lines as close as possible to each chip and 1 – 100 µF tantalum capacitors common for all chips on a PCB. Use 100 nF on the *mbias* (and eventually other biases that are externally generated) close to the chip.

6.3 Control register (to be updated)

The VATAGP7 has an approximately 920 bit long control register, set by *regin* and *clkin*. Typical contents of the register is shown below.

Bit [1)]	Name	Function	Comment
1	Vrc select	Select which internal Vrc value to use	0 → 0.7 V (pos. sig.) 1 → 0.9 V (neg. sig.)
2	Vfsf select	Select which internal Vfsf value to use	0 → -125 mV (pos. sig.) 1 → -255 mV (neg. sig.)
3	Vfss select	Select which internal Vfss value to use	0 → -75 mV (pos. sig.) 1 → -135 mV (neg. sig.)
4	Vfp select	Select which internal Vfp value to use	0 → -610 mV (pos. sig.) 1 → -550 mV (neg. sig.)
5	cc_enable	Enable current compensation (CC)	0 → CC off 1 → CC on
6	n_side	Readout of n-side of the detector (integrating	0 → p 1 → n

Bit [1)]	Name	Function	Comment
		electrons).	
7	test_on	Test mode on	0 → test off 1 → test on
8	select	Select signal polarity	0 → positive 1 → negative
9:12	addr[10:7]	chip address	
13	Threshold High level	Vthrhc = +1.5V/-2V	0 → AVSS 1 → AVDD
14	calc	Calibration ctrl	0 → internal cal. Step 1 → external generation.
15	Vrc_neg select		0 → positive 1 → negative
16	Reserved.		Set to 0.
17	Slew_on	Bit for turning on the fast shaper slew rate	0 → off 1 → on
18	reserved		
19	dltc	Disable late trigger (DLT)	0 → DLT active 1 → DLT inactive
20:147	Threshold Norm/High	Disable channel (vthrh = +1.5V/-2V)	0 → enable (norm) 1 → disable (high/vthrh)
148:659	DAC[4:0] for ch[0:127]	Threshold DACs	
660	test_enable for test channel	Enable injection of cal-pulse into test channel	0 → disable 1 → enable
661:788	test_enable for ch[0:127]	Enable injection of cal-pulse into channel	0 → disable 1 → enable
789	reserved		
790:794	inp_drain for ch[0:127]	Enable charge draining of noisy channels.	0 → disable 1 → enable

1) Bit number in the control register. Bit 1 is the first bit after *regin*, bit 794 is the last bit before *regout*. Reverse the order when downloading the bit stream (download bit 794 first and bit 1 last).

6.4 Threshold High level

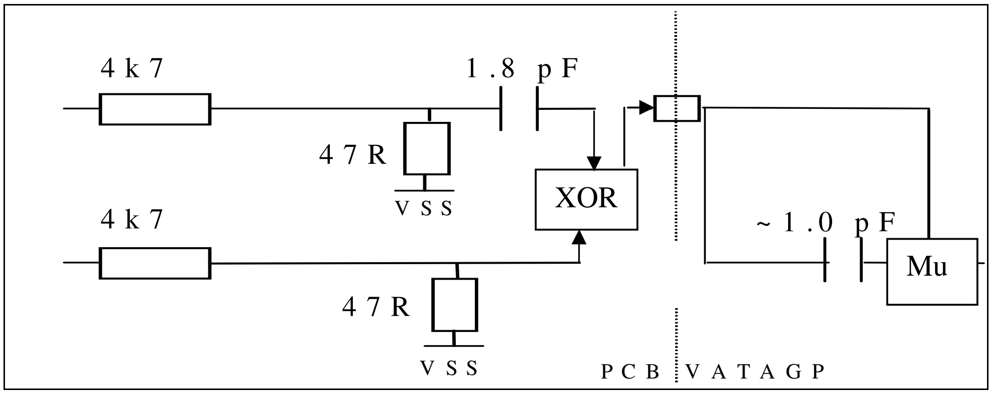
This bit is used to activate or deactivate the discriminator, i.e. setting *vthrhc* high would set *vthrh* to AVDD. This would activate the discriminator and disable the corresponding channel, given the channel disabling threshold norm/high (see 6.7) is set high. Otherwise, the discriminator is deactivated and lets any input signal pass through, given the channel disabling threshold norm/high (see 6.7) is set high.

6.5 ASIC test and calibration

Each channel can be individually tested. This function is enabled by setting bit *test_on* in the control register to “1”. The *test_enable* mask must have one of its bits set to “1” which will select the corresponding channel (selecting more than one channel is possible due to AC coupling on the inputs but is not expected to be very useful). The channel(s) that has been selected will be sensitive to test-signals injected at the *cal* inputs.

When choosing externally AC coupled input signal, place the 1.8 pF capacitor very close to the chip to prevent pickup. Otherwise, there is a ~1.0 pF internal capacitor on the chip.

A voltage step of 10 mV on the 1.8 pF capacitor gives an input signal charge of 18 fC (~5 MIP).



6.5.1 Internal test circuitry

We will implement an internal cal-pulse generator based on Carlo's proposal. It is based on an internal DAC, and an external digital calibration trigger. The calibration trigger can be connected to the external pad *cale*.

The cal-dac will have 4 bits. Each setting corresponds to the following table:

Bit1	Bit2	Bit3	Bit4	Cal pulse [fC]
0	0	0	0	18
0	0	0	1	15.75
0	0	1	0	13.5
0	0	1	1	11.25
0	1	0	0	9
0	1	0	1	6.75
0	1	1	0	4.5
0	1	1	1	2.25
1	0	0	0	18
1	0	0	1	20.25
1	0	1	0	22.5
1	0	1	1	24.75
1	1	0	0	27
1	1	0	1	29.25
1	1	1	0	31.5
1	1	1	1	33.75

Table 3: The relationship between the CAL-DAC and the cal-pulse.

6.5.2 Test channel

This ASIC is equipped with a test channel for monitoring the fast shaper output. It has a dedicated probe pin for this purpose. You can either apply a signal directly to the input through an input pad or through the cal. input. The input draining feature can also be tested on this channel.

6.6 Threshold Norm/High

This bit chooses between a normal threshold and a disabling high threshold. However, the high threshold level could be chosen to be a transparent level, e.g. does not discriminate any signal.

6.7 Dlt (Disable Late Trigger)

The Dlt circuit of the ASIC has both a driver and a sense function. This enables the possibility for disabling late triggers between several interconnected ASICs. The sense circuit is a simple comparator while the driver has an open-drain configuration which requires external termination.

NB! The Dltc-bit in the control register disables the driver, not the sense-comparator.

The figure below shows a typical way of terminating the Dlt:

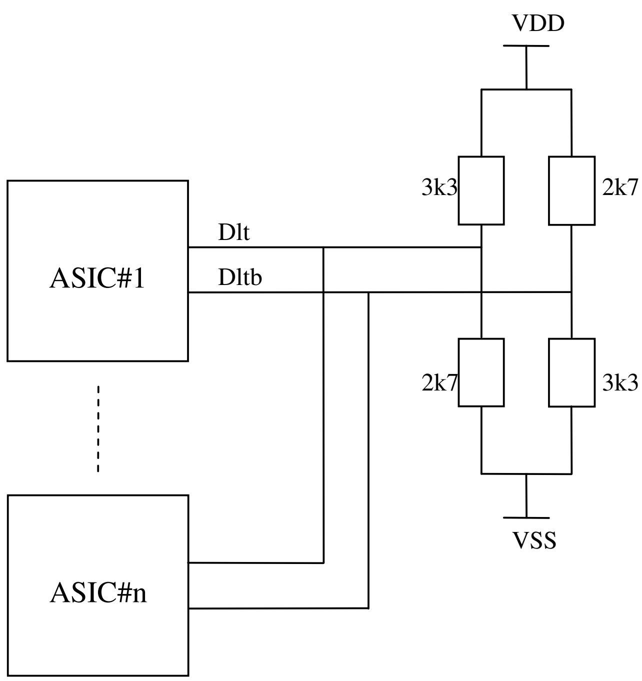


Figure 4: Dlt termination

6.8 Channel threshold DACs

The channel threshold DACs has nominally 1 mV step size. The step size can be changed by forcing a different *ref_bi*. The step size in [mV] is **ref_bias[uA] * 0.1.** The DAC is sink-source type, and will ideally leave no return current in the threshold line.

DAC0	DAC1	DAC2	DAC3	Threshold adjust (ref_bias=10uA)
0	0	0	0	0 mV
0	0	0	1	-1 mV
0	0	1	0	-2 mV
0	0	1	1	-3 mV
0	1	0	0	-4 mV
0	1	0	1	-5 mV
0	1	1	0	-6 mV
0	1	1	1	-7 mV
1	0	0	0	0 mV
1	0	0	1	1 mV
1	0	1	0	2 mV
1	0	1	1	3 mV
1	1	0	0	4 mV
1	1	0	1	5 mV
1	1	1	0	6 mV
1	1	1	1	7 mV

6.9 Global threshold DAC

This DAC is for trimming the global threshold. This could also be used to even out offset currents that are generated when the channel DACs have been adjusted. Therefore, this DAC has the same current step-size as the channel DACs.

NB! For this DAC to work an external resistor has to be placed on the threshold line. The step in mV will be: **Rext * 2.5 µA.**

DAC0	DAC1	DAC2	DAC3	DAC4	Threshold adjust (ref_bias=10uA)
0	0	0	0	0	0 mV
0	0	0	0	1	-2.5 µA * Rext
0	0	0	1	0	-5.0 µA * Rext
0	0	0	1	1	-7.5 µA * Rext
0	0	1	0	0	-10.0 µA * Rext
0	0	1	0	1	-12.5 µA * Rext
0	0	1	1	0	-15.0 µA * Rext
0	0	1	1	1	-17.5 µA * Rext
0	1	0	0	0	-20.0 µA * Rext
0	1	0	0	1	-22.5 µA * Rext
0	1	0	1	0	-25.0 µA * Rext
0	1	0	1	1	-27.5 µA * Rext
0	1	1	0	0	-30.0 µA * Rext
0	1	1	0	1	-32.5 µA * Rext
0	1	1	1	0	-35.0 µA * Rext
0	1	1	1	1	-37.5 µA * Rext
1	0	0	0	0	0 mV
1	0	0	0	1	2.5 µA * Rext
1	0	0	1	0	5.0 µA * Rext

1	0	0	1	1	7.5 µA * Rext
1	0	1	0	0	10.0 µA * Rext
1	0	1	0	1	12.5 µA * Rext
1	0	1	1	0	15.0 µA * Rext
1	0	1	1	1	17.5 µA * Rext
1	1	0	0	0	20.0 µA * Rext
1	1	0	0	1	22.5 µA * Rext
1	1	0	1	0	25.0 µA * Rext
1	1	0	1	1	27.5 µA * Rext
1	1	1	0	0	30.0 µA * Rext
1	1	1	0	1	32.5 µA * Rext
1	1	1	1	0	35.0 µA * Rext
1	1	1	1	1	37.5 µA * Rext

7 Readout modes

The VATAGP7 has three different readout modes. After the physics event, each preamplifier will integrate its eventual signal. The slow shaper will shape the signal with a shaping time of 3us, and the fast shaper with a shaping time of 1us. If the signal of the fast shaper has a value larger than the external threshold (*vthr* or *vthr_h*), a trigger on the *to*/*tob* and *mgo* lines occur. When the slow shaper reaches the signal peak (nominally after 3 µs), the external hold signal (*sh*/*shb*) should be applied to sample the peak value. Immediately after this, the readout can start.

7.1 Mode 1: Serial readout

Readout is similar to the VA+TA type of ASICs from Gamma Medica-Ideas.

A shiftregister will enable readout of one channel at a time. The readout starts with clocking one bit into the first channel of the shiftregister with the *shift_in_d* and *gck*/*gckb* signals. See Figure 5 for an example of the timing in this mode. The logic part of the chip can be reset either by applying the *res/resb*, or by running through the full read-out sequence (more than 128 clocks) so that the last shift bit is clocked out of the register.

On power-up, a reset signal should be applied to reset the internal registers/latches with a pulse (~1 µs- 1 ms) on the *res*/*resb* lines. Eventually, a number of clocks exceeding the number of channels will set the shiftregister to zero.

In this mode, the following input signals are not in use and can be left unconnected:

shift_in_u	(internal pull down)
shift_out_u	
shiftreg	(internal pull up)
shiftregb	(internal pull down)
vi	(internal pull down)
vib	(internal pull up)
vo	
vob	

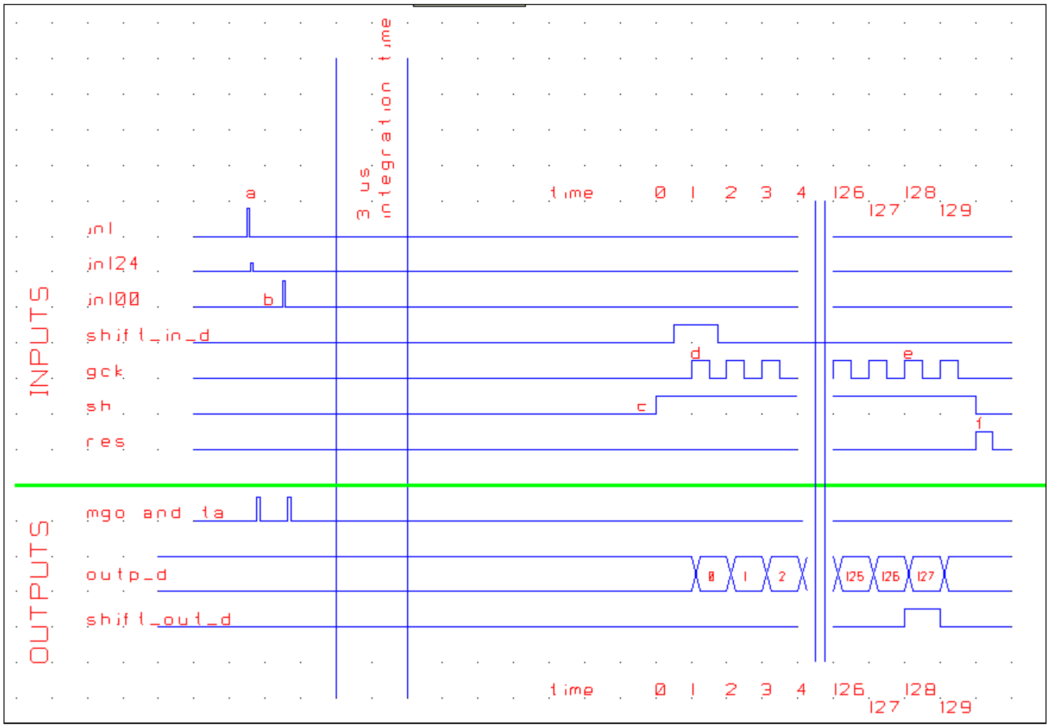


Figure 5: Serial readout

a) Physics events happen almost simultaneously in channel 1 and 124. Since the signal is larger than the threshold, a trigger (*mgo*, *ta*/*tb*) is generated. The fast shaper for the trigger logic has a shaping time of 50 ns, which means that dependent of the signal amplitude and the threshold *vthr*, the trigger can be delayed up to 50 ns.
b) Another physics event happen some time later in channel 100. This event also generates a trigger.
c) After 500ns, the sample-and-hold signal *sh*/*shb* goes high. The signal in channel 1 and 124 has reached the peak, while channel 100 has not fully reached the peak yet.
d) A shift bit is clocked into the shiftregister by *shift_in_d* and *gck/gckb*. The analogue value of channel 0 is enabled at *outp_d/outm_d*. For each clock (*gck/gckb*), the shiftbit is clocked to the next channel.
e) The last channel is enabled. The *shift_out_d* goes high to give a *shift_in* for the next chip in the chain.
f) A reset is applied to reset the shiftregister. This is not necessary if all channels have been clocked, so that the shift bit has been clocked out of the chip.

7.2 Mode 2: Sparse readout

In this readout mode, only the channels with a trigger (signal above the threshold) will be read out to increase the readout speed. As in serial readout, the hold signal *sh/shb* must be applied 500 ns after the trigger.

If Dlt is deactivated all channels with a trigger will get a read tag. By clocking once with the *gck/gckb*, the analogue value and the address of the first channel with a tag will be available on the output. After the next clock of *gck/gckb*, the next channel with a tag will be available. The *vo* signal goes low when all channels with triggers are read out. If the chip shall be reset before all channels are read out, apply the *res/resb* signal.

In this mode, the following input signals are not in use and can be left unconnected:

shift_in_u	(internal pull down)
shift_out_u	
shift_in_d	(internal pull down)
shift_out_d	

These signals have a fixed level:

vi (chip 0)	connect to VSS (logic low)
vib (chip 0)	connect to VDD (logic high)
shiftreg	connect to VSS (logic low)
shiftregb	connect to VDD (logic high)

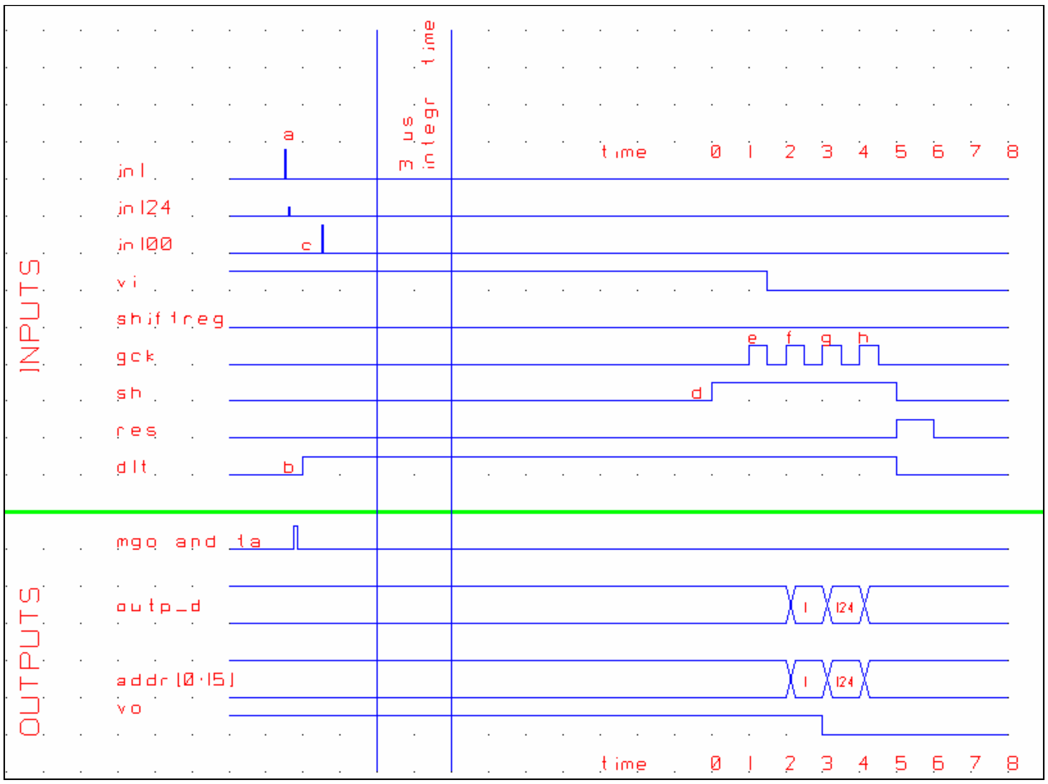


Figure 6: Sparse readout

a) Physics events happen almost simultaneously in channel 1 and 124. Since the signal is larger than the threshold, a trigger (*mgo*, *ta*/*tb*) is generated. The fast shaper for the trigger logic has a shaping time of 50ns, which means that dependent of the signal amplitude and the threshold, the trigger can be delayed up to 50ns.
b) The disable_late_trigger *dlt* is applied. This will discard all triggers after this moment.
c) Another physics event happen some time later in channel 100. No trigger is given because *dlt* is high.
d) After 500ns, the sample-and-hold signal *sh*/*shb* goes high. The signal in channel 1 and 124 has reached the peak and are held.
e) The *gck/gckb* clocks once. Since veto in *vi* from the previous chip in the chain is high, no action is taken.
f) The *gck/gckb* clocks once. Veto in *vi* is low, and the first channel with a hit is enabled at the output together with its address.

g) The next and last channel with a hit is enabled at the output together with its address. Veto out *vo* goes low to indicate that all channels are read out and enable readout of the next chip in the chain.
h) *Sh* and *dlt* goes low. A reset is applied to reset the shiftregister by a pulse on *res/resb*. This is not necessary if all hit channels have been clocked, so that the veto out in the last chip has gone low.

7.3 Mode 3: Sparse readout with neighbour channels

This mode is equal to the sparse readout, except that the neighbours of the channel(s) with trigger can also be read out.

As in serial readout, the hold signal *sh/shb* must be applied 500ns after the trigger.

If Dlt is deactivated all channels that trigger will get a read tag. By clocking once with the *gck/gckb* and with *shiftreg* low, the analogue value and the address of the first channel with a tag will be available on the output. By setting *shiftreg* high and clocking more clocks, the neighbours of the trigger channel will be available.

Be setting *shiftreg* low and giving another clock of *gck/gckb*, the next channel with a trigger will be available.

All channels with triggers are read out when the *vo* goes low. If the chip shall be reset before all channels are read out, apply the *res/resb* signal.

These signals have a fixed level:

vi (chip 0)	connect to VSS (logic low)
vib (chip 0)	connect to VDD (logic high)

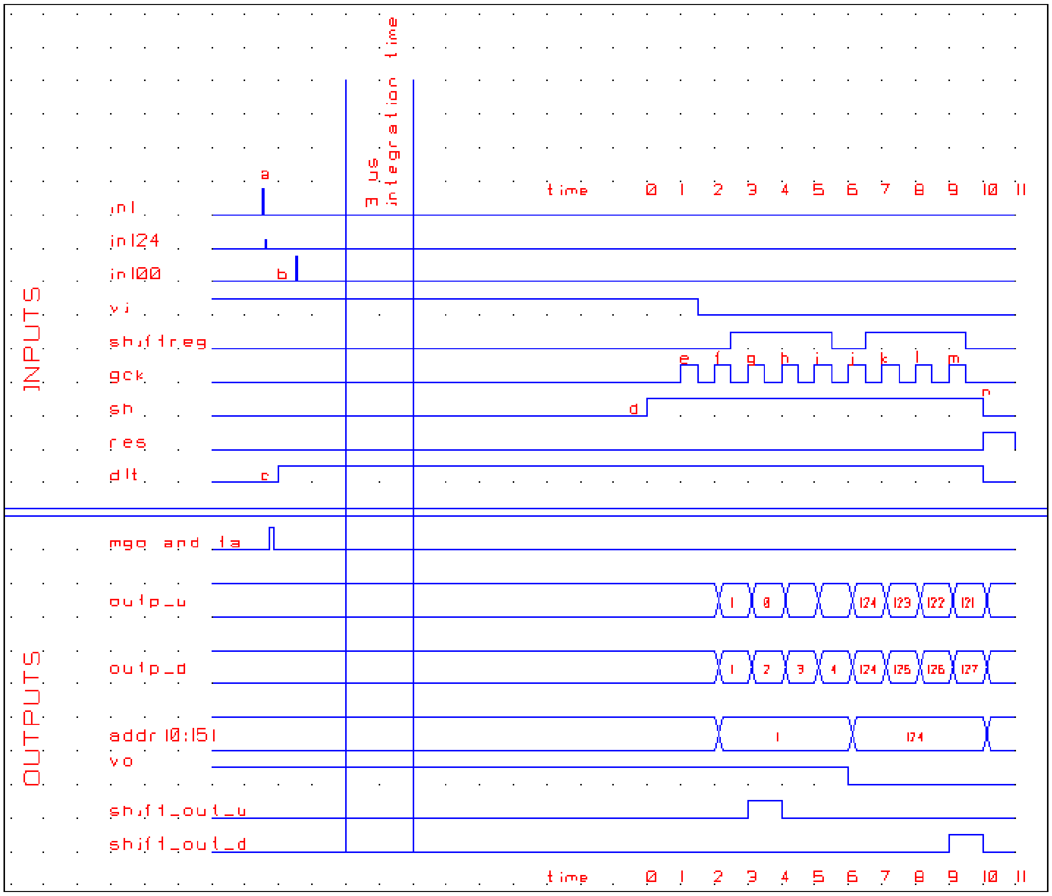


Figure 7: Sparse readout with neighbour channels

a) Physics events happen almost simultaneously in channel 1 and 124. Since the signal is larger than the threshold, a trigger (*mgo*, *ta*/*tb*) is generated. The fast shaper for the trigger logic has a shaping time of 50ns, which means that dependent of the signal amplitude and the threshold, the trigger can be delayed up to 50ns.
b) The disable_late_trigger *dlt* is applied. This will discard all triggers after this moment.
c) Another physics event happen some time later in channel 100. No trigger is given because *dlt* is high.
d) After 500ns, the sample-and-hold signal *sh/shb* goes high. The signal in channel 1 and 124 has reached the peak and are held.
e) The *gck/gckb* clocks once. Since veto in *vi* from the previous chip in the chain is high, no action is taken.
f) The *gck/gckb* clocks once with *shiftreg* = low. Veto in *vi* is low, and the first channel with a hit is enabled at the output together with its address.
g) The *gck/gckb* clocks once with *shiftreg* = high. The analogue values of the two next neighbour channels of the hit channel are read out on the *outp_u/outm_u* and *outp_d/outm_d* lines.
h) Same as g)
i) Same as g)
j) The *gck/gckb* clocks with *shiftreg* = low. The next channel with a hit is enabled at the output together with its address.
k) Same as g)

l) Same as g)
m) Same as g)
n) The chip is reset by setting *sh* and *dlt* low and by giving a short *res/resb* pulse.