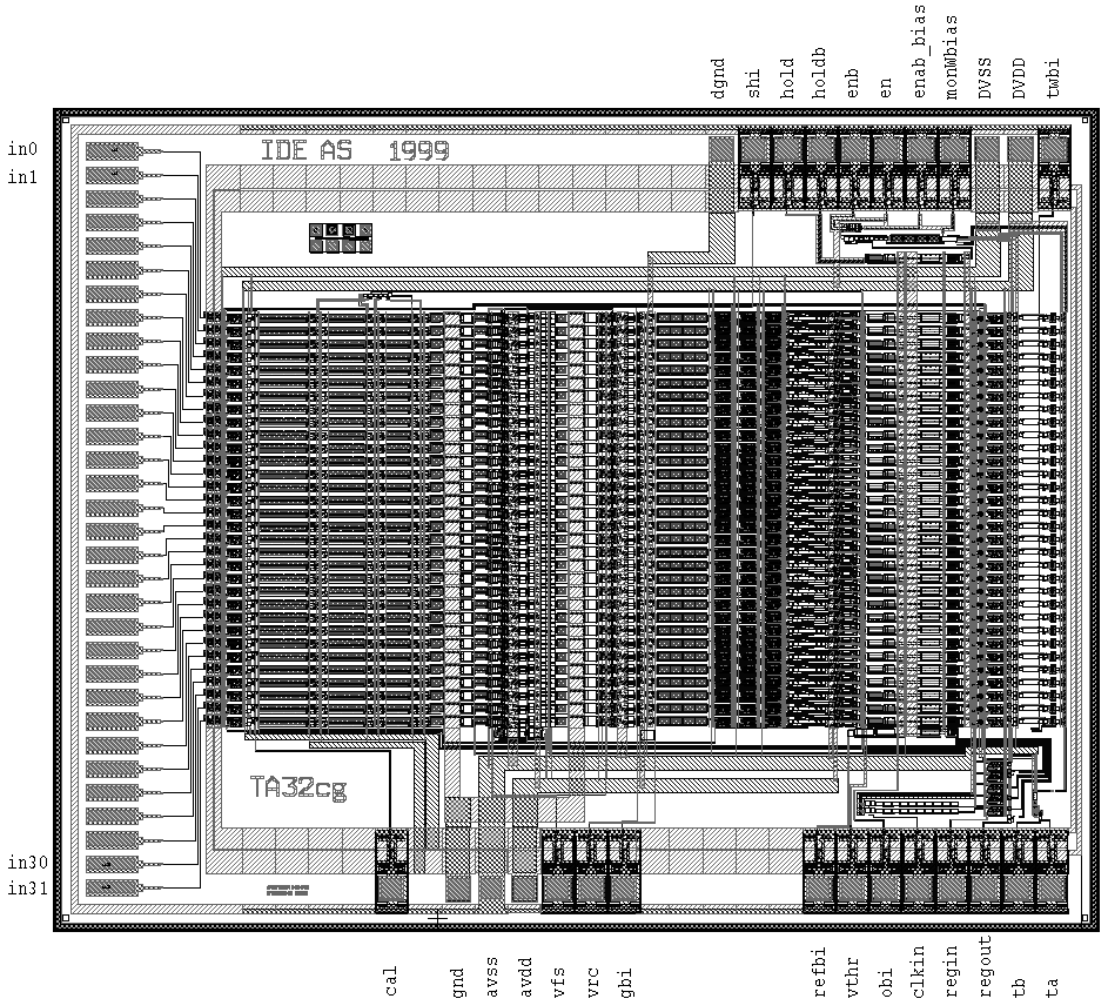
TA32CG

Description



Tel.: + 47-67 55 18 18 Fax.: + 47-67 55 96 30
E-mail: ide@ideas.no Homepage: www.ideas.no

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1. General

- Description:

  32 channel low power fast triggering ASIC to be used with a matching VA circuit in the front (see VA documentation). The chip includes for each channel a fast CR-RC shaper followed by a level-sensitive discriminator. The trigger signals from each channel are wire-or'ed together onto one common trigger output. To reduce threshold-spread, this version has a (switchable) higher gain than it's presuccessor (VA32C) and it also has trim-DAC's on each discriminator.

- Can be used with:

  Presently: VA32C, VA32_hdr2 (other variants can be made and may be available later)

- Vendor:

  Integrated Detector & Electronics AS (IDE AS),
  Veritasveien 9, 1322 Høvik, Norway.

  For Sales and Customer Support please contact:

  Phone: +47-67 55 18 18
  Fax: +47-67 55 96 30
  e-mail: ide@ideas.no , http://www.ideas.no

- Availability:

  Available as unpackaged, wafer tested dices or mounted on hybrids (dedicated or standard designs). Normally stock goods.

2. Physical

- Process: 1.2 µm N-well CMOS, double-poly, double metal.

- Die size: 4410 µm x 3480 µm (including scribe)
  Thickness: ~ 600 µm

- Input bonding pads: Single row.
  Pad size: 50 µm x 200 µm
  Pad pitch: 100 µm (see. Fig. 2)

- Output, control and power pads: Single row.
  Pad size: 90 µm x 90 µm
  Pad pitch: 140 µm (see fig. 2)

3. Electrical

Power rails:	Vdd = +2 V, Vss = -2 V Each with separate connections for analog (avdd and avss) and digital sections (dvdd, dvss) of the chip.	
Back contact:	metalized, connect to avss (-2V)	
Current description: (Quiescent, typical values)	dvdd dvss avdd avss gnd	~ 3 mA ~ 3 mA ~ 1.5 mA ~ 8 mA ~ 6.5 mA
Input bias currents: (*sbi*, *refbi* and *obi* driven to devices (e.g. resistors) referred to vdd, *twb* and *gbi* to vss)	Nominal values sha_bias (*sbi*): 120µA ota_bias (*obi*): 90µA TrigWbias (*twbi*): 10µA GstageBias (gbi): 200µA DACreference (refbi): 20µA	
Peaking time shaper:	Nominal: Adjustable:	75 ns 75 ns – 150 ns
Power dissipation: (Typical values)	Quiescent:	~ 30 mW (0.9 mW/channel)
ESD Protection:	Inputs: none Control: ~ 300Ω series resistor and protection diodes to Vdd and Vss.	
Input stage (Shaper):	Input device: PMOS referenced to gnd Signal input potential: ~ -1.2 V to –1.3 V	

4. Power-, Bias- and Control- Pad Description

Top row, from left (see chip plot on next page (Fig.1.))

Pad name	Type	Description	Nominal value
dgnd	p	Ground	0 V
sbi	ai	Bias current for shaper-amplifiers.	120 µA
hold	di	*)	Logical (vdd☼)
holdb	di	*)	Logical (vss☼)
enb	ao	**)	Current (vdd☼)
en	ao	**)	Current (vdd☼)
enab_bias	ai	***)	20µA (vdd☼)
monWbias	ai	***)	20µA (vdd☼)
dvss	p	digital vss	-2 V
dvdd	p	digital vdd	+2 V
twbi	ai	Bias adjust for trigger width	10 µA

Bottom row, from left

Pad name	Type	Description	Nominal value
cal	ai	Calibration input	voltage step
gnd	p	Ground	0 V
avss	p	Analogue vss (+ chip backplane)	-2 V
avdd	p	Analogue vdd	+2 V
vfs	ai	Control voltage for feedback resistor (NMOS) in shaper	700mV
vrc	ai	Control voltage for High-pass filter resistor (NMOS) in front of Discrim.	1.4V
gbi		Bias for gain-stage	200µA
refbi		Bias for trim-DACs	20µA
vthr	ai	Discriminator threshold	± 50mV (e.g)
obi	ai	Bias current to Discriminator	90 µA
clkIn	di	Clock Input for disable register	Logical
RegIn	di	Input to the disable register	Logical
regout	do	Output of the disable register	Logical
tb	ao	Trigger out inverted	current
ta	ao	Trigger out	current

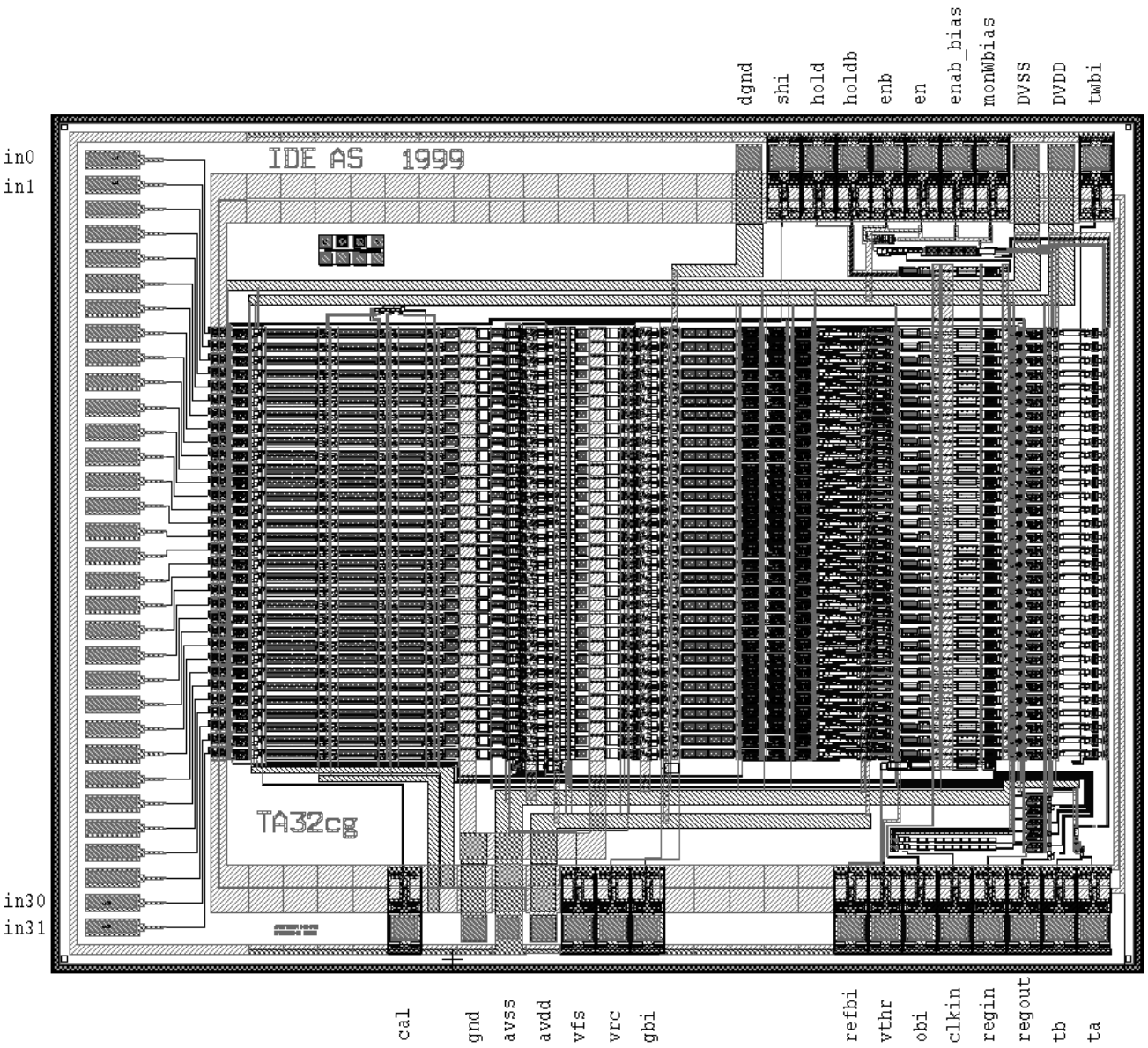
p = power, di = digital in, do = digital out, ai = analog in, ao = analog out
Logical = +2V (“1”) / -2V (“0”)

If the “selective chip function” (see chapter 5) is used together with the VA32C.2 chip (another IDE product) these signals are:

*) the same as those applied to the VA.
**) to be connected to the signals with the same name on the VA
***) Bias currents

☼ If “selective chip function” not used (see chapter 5)

The TA32CG circuit



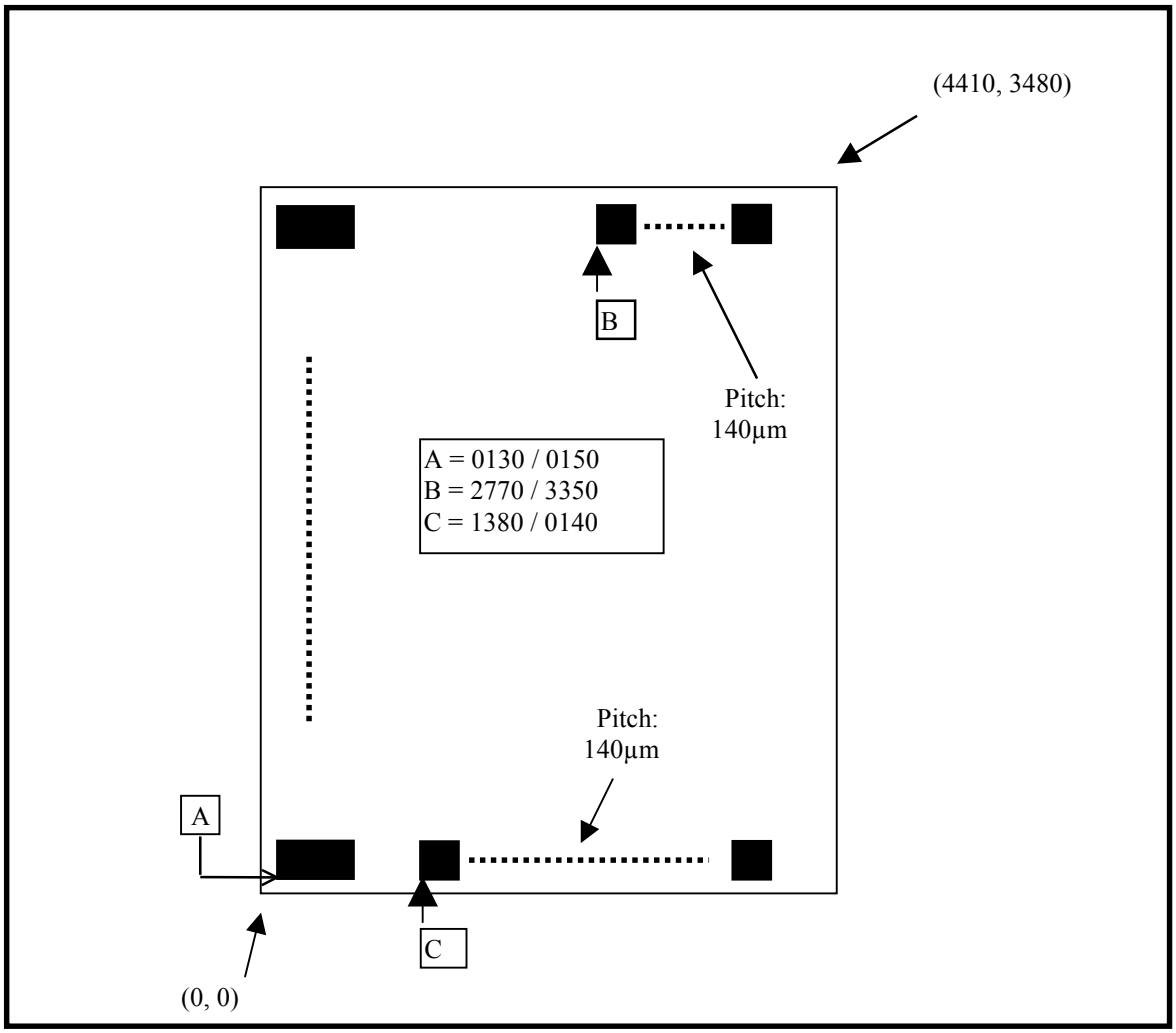


Fig. 2 Chip geometry & pad placement (Not to scale - all dimensions in µm. Please note that the referred co-ordinates are layout co-ordinates. Add 50 µm -100 µm on each side for scribe/cutting tolerances).

5. Functional Description

The TA32cg is useful only together with a VA32xx[1] chip placed in the front. The concept is (see Fig.4) that TA32cg and VA32xx share the same preamplifier which is located on the VAxx i.e. the inputs of TA32cg is directly coupled to corresponding outputs of these preamplifiers.

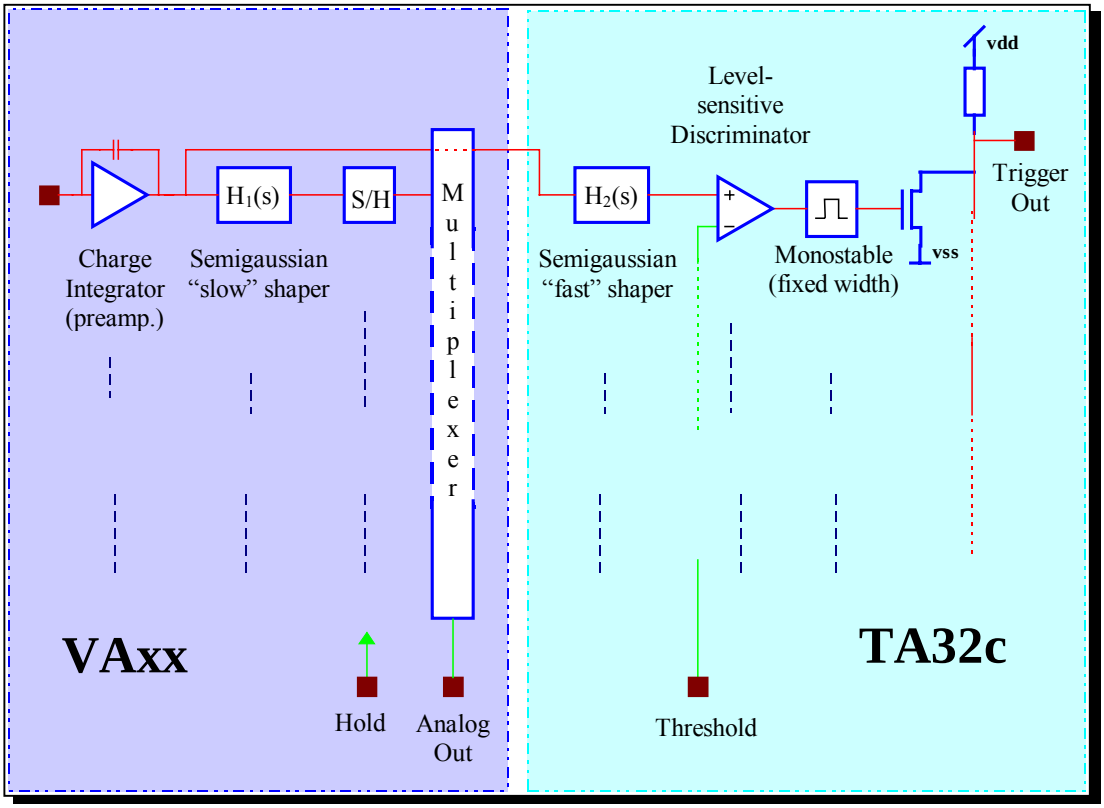


Fig 4. The VA-TA principle

As shown in Fig.5 the TA32cg chip consists of 32 identical parallel channels. Each channel includes a (optional) switchable gain-stage followed by a fast CR-RC 75ns shaper which again is followed by a level-sensitive discriminator. The discriminator is preceded by a High-Pass filter (not shown) with a very low cut-off frequency in order to reduce offset-spread across chip. Each discriminator has individual offset adjustment that can be programmed through 3bit DACs located on the negative input of each discriminator (see later for explaination).

[1] Not all VA32xx circuits are suitable. Please contact us for questions related to this.

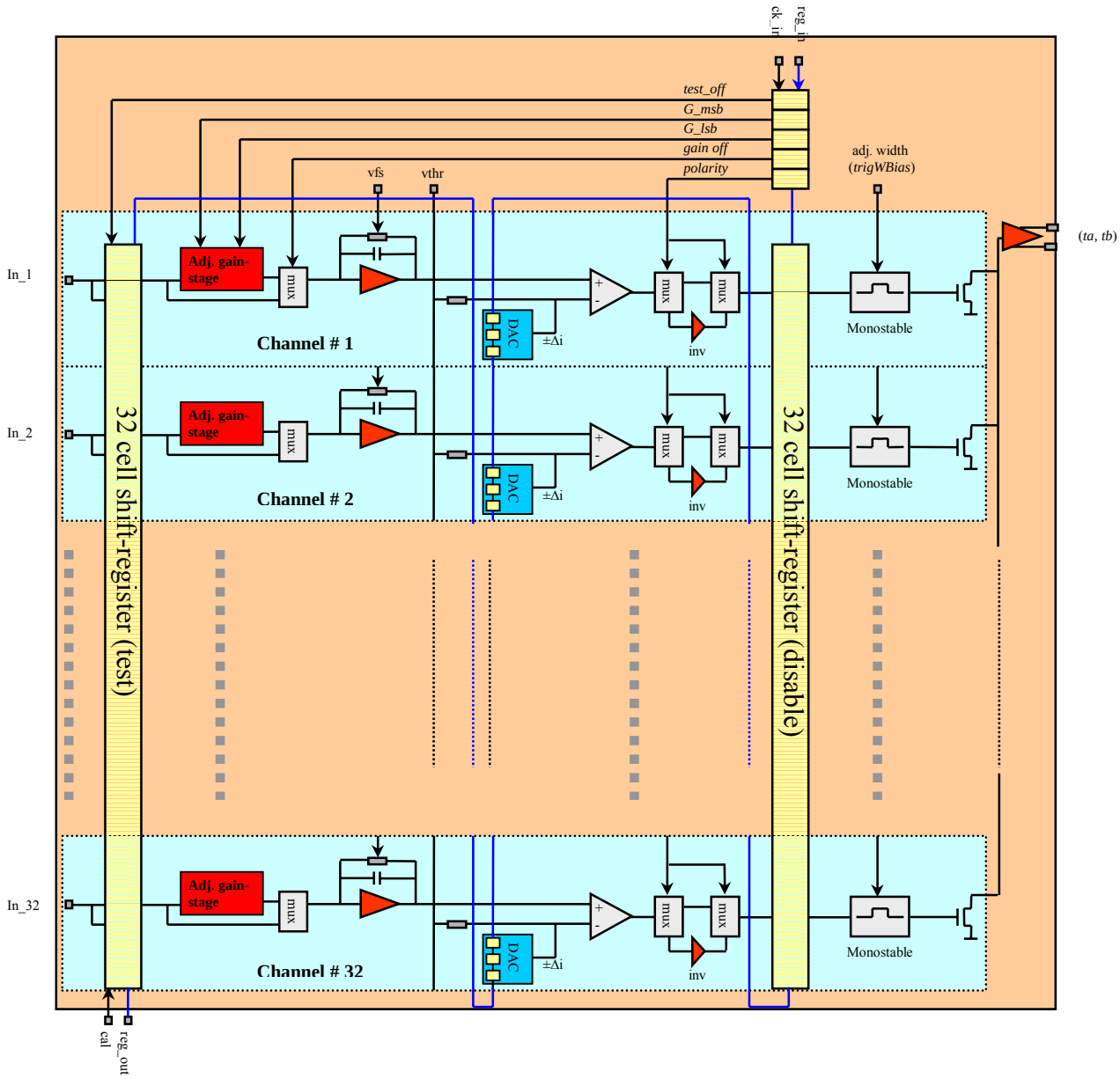


Fig 5. TA32CG Architecture

Following the discriminator, which threshold is externally adjustable (***vthr***), is a circuitry which makes it possible to select between usage for positive or negative input signals.
Following this circuitry is an edge-trigged monostable flip-flop that gives a fixed pulse-width which is externally adjustable (***trigWbias***). At the end of the channel is a pull-down transistor that serves as one input to all 32 channel wire-or circuitry. Whenever a signal in any of the channels is rising above the discriminator threshold the wire-or'ed output will cause a chip-global trigger output on $\mathbf{t_a}$ and $\mathbf{t_b}$.

Down-loadable control parameters:

The chip includes a 161 bit serial shift-register (data = ***RegIn,*** clock = ***ClkIn***) where the function of the first down-loaded 32 bits is to select a channel for individual channel testing (test-mask). The next 3x32 bits are for the threshold DACs (dac-mask). The following 32 bits has the function of a disable-mask i.e. a "1" in one of the bits will disable the corresponding channel. The last 5 bits are chip mode-settings (chip-mode mask) used to #1 select signal-polarity #2 disable the gain-stage #3 MSB of the gain-setting #4 LSB of the gain-setting and #5 set the chip in test-mode (used together with the test-mask).

The DACs:

The offset change in the discriminators are simply accomplished by adding or subtracting a current over a resistor. The reference current is adjustable and set by the ***refbi*** bias (nominally 20 µA). Currents are added/subtracted by changing the bitpattern in the 3x32bit dac-mask. The following table shows the relations between the individual 3bit bitpattern of each DAC and the change in offset value. Bit1 is the first bit in the down-load stream.

Bit1	Bit2	Bit3	Offset change (mV)
0	0	0	None
0	0	1	- ½ * 0.1 * refbi (µA)
0	1	0	- 1 * 0.1 * refbi (µA)
0	1	1	- 1½ * 0.1 * refbi (µA)
1	0	0	None
1	0	1	+ ½ * 0.1 * refbi (µA)
1	1	0	+ 1 * 0.1 * refbi (µA)
1	1	1	+ 1½ * 0.1 * refbi (µA)

Be aware that if the netsum of the ± currents is non-zero, a common term offset will occure.

The switchable gain-stage:

This stage is by default used. It can be switched off by down-loading a "1" into bit #2 of the chip-mode mask. If the gain-stage is on, the signal will appear non-inverted on the 75ns shaper output but it will be inverted in case of gain-stage off.

The gain is set by changing bit #3 and #4 in the chip-mode mask. The relation is as follows:

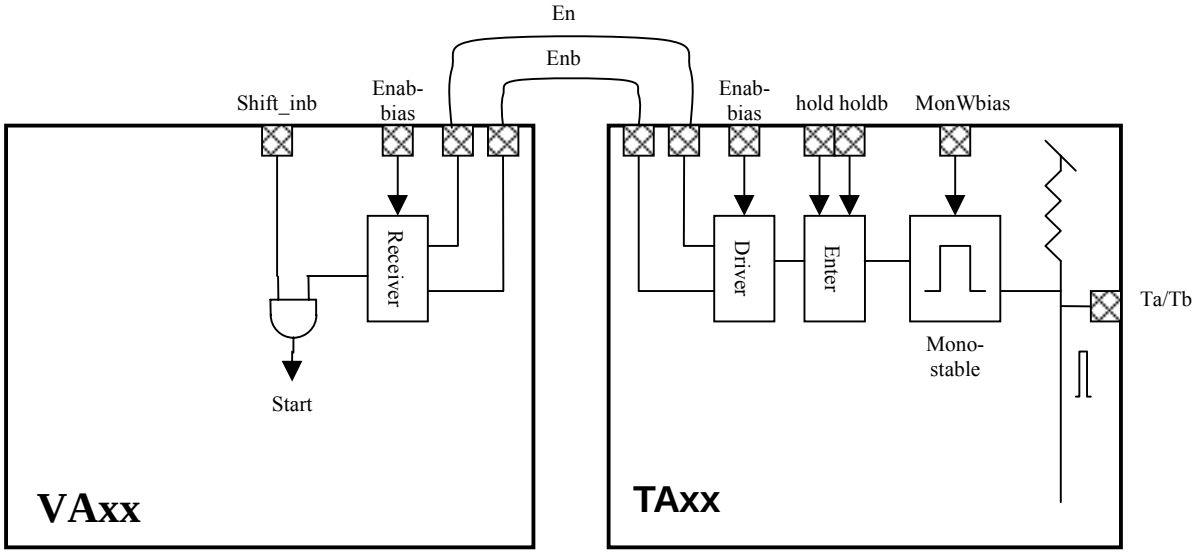
Bit#3	Bit#4	Gain
0	0	1x
0	1	3x
1	0	6x
1	1	10x

The Test function:

Each channel can be individually be tested. This function is enabled by setting bit #5 in the chip-mode mask to "1". The test-mask must have one of it's bits set to "1" which will select the corresponding channel (selecting more than one channel is possible due to AC coupling on the inputs but is not expected to be very useful). The channel(s) which has been selected will be sensitive to test-signals injected at the cal input. Unlike most cal-functions in the VA circuits, this chip is voltage edge sensitive and the test-pulse should consequently be a voltage-step, positive or negative. The duration of the pulse should be minimum 1µs.

The "selective chip" function:

A special feature that optionally exists is to automatically select only the chip (in a daisy-chain) that actually is the chip that is triggering for the given event. By inteconnecting the TA32cg and VA32c in the manner shown below, the flag generated in the TA32cg (and which has a duration adjustable by ***MonWbias***) will be transferred to the VA32c at the moment of the Sample/Hold (***hold/holdb***). Thus, only the VA32c chip that has this flag transferred will be sensitive to shift_inb and only this chip will consequently be read out.



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