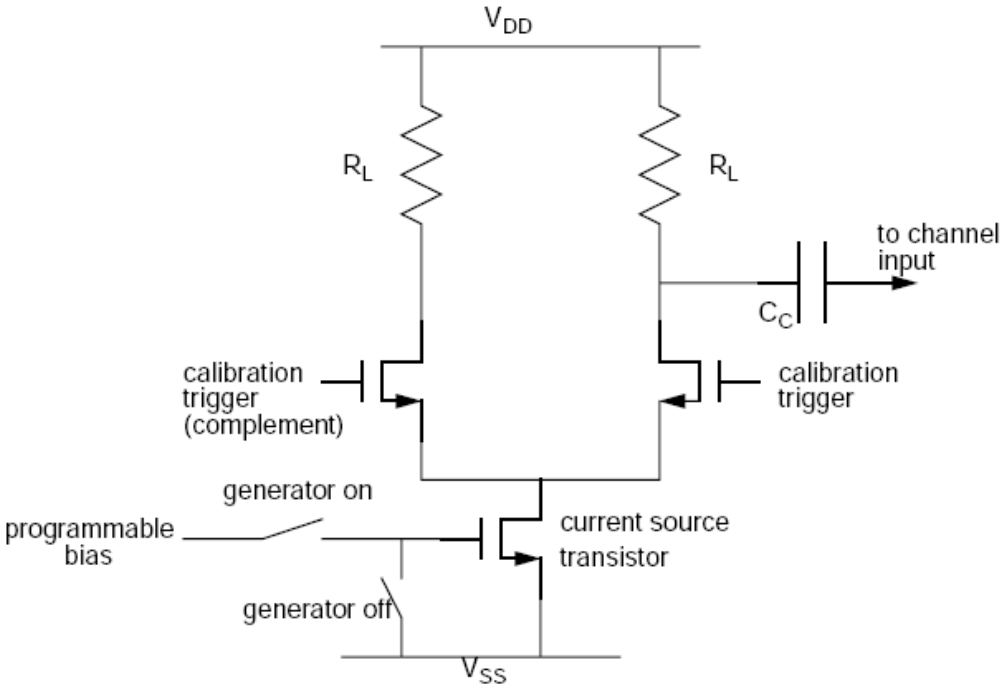
Proposal for an internal calibration circuit.

We would like to have a programmable internal calibration pulse instead of having to supply a very small voltage step with the corresponding amplitude or adding voltage dividers all over the place. The drawback of the current implementation is that the calibration pulse picks up a lot of noise in its way to the chip.

What we propose here is to have the pulse generated inside the chip with a programmable amplitude. Sindre wanted to still keep the current method. I believe this can still be done in the following mode:

- Leave *cali* input pad as it is now, so that you inject there the voltage step with the proper amplitude and the internal capacitor converts that to a current pulse.
- Change *cale* to accept a calibration trigger. A trigger signal there will start the internal calibration procedure.

The internal calibration could be implemented as sketched in the following picture which shows what the CMS people have done for the APV25 ASIC:



The thing would be implemented as a differential pair with resistive load R_L to convert the calibration trigger into a voltage step. The trigger signal and its complement switch on one transistor and turn off the other one in the differential pair, causing the bias current to switch from one branch to the other. When it switches to the output branch, it moves from VDD to VDD-$I_{CAL}R_L$, stepping back to VDD when the current is switched back to the other branch. The current source transistor is biased by a programmable voltage. The output after the calibration capacitor would then join the VATA circuit in the same place as the old *cale* was.

The value for the programmable voltage could be programmed in the configuration register.

This way we maintain the current pad layout and add this new feature to the chip. The choice *cali* and *cale* here is arbitrary. One could change that and "save" the internal capacitor of *cali* if this can be an issue