SEU studies of the upgraded BELLE vertex detector FEE

Samo Korpar
University of Maribor and Jožef Stefan Institut

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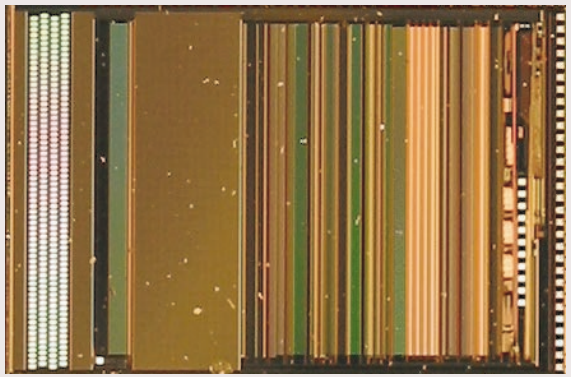
1. Motivation
2. Setup
3. Measurements
4. Summary and plans

VA1TA characteristics

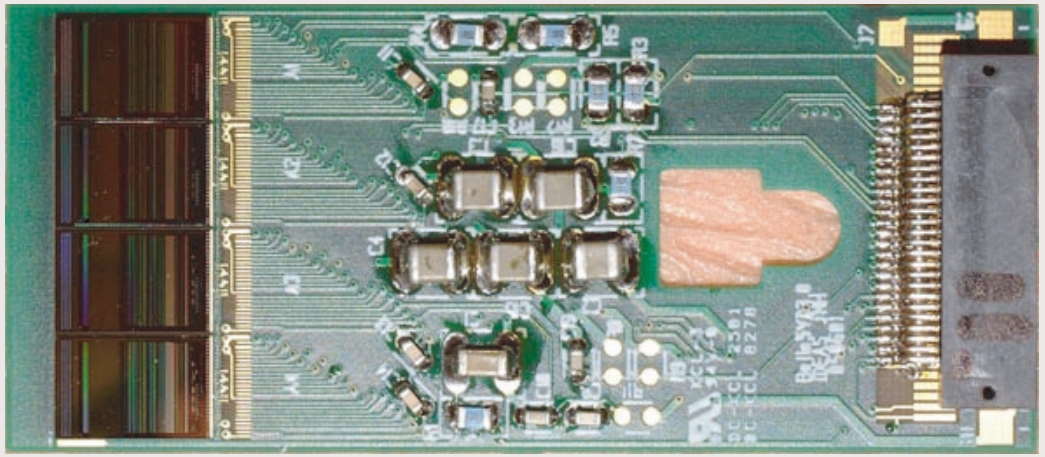
The readout of the upgraded vertex detector is based on the VA1TA chip:

- channels: 128
- readout: multiplexed analog
- bias: all biases internally generated from single external current bias
- process: 0.35 μm N-Well CMOS,double-poly, triple metal with epitaxial layer
- die size: 9.28 mm $\times$ 6.12mm
- thickness: $\approx$ 725 μm

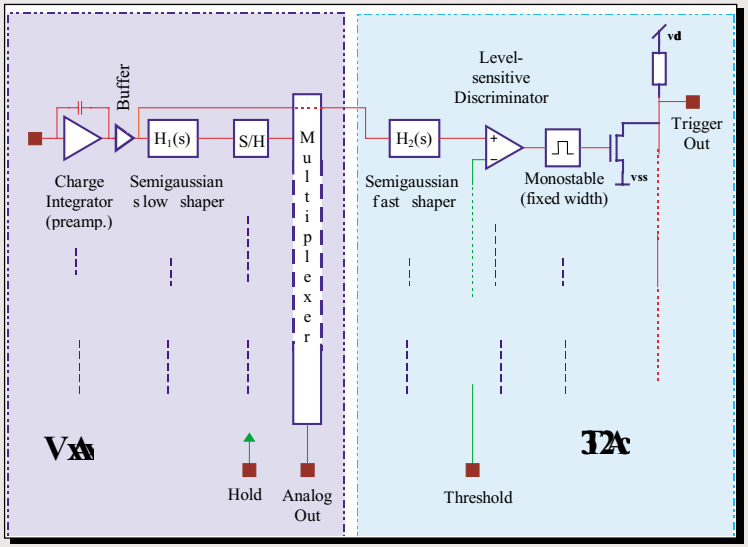


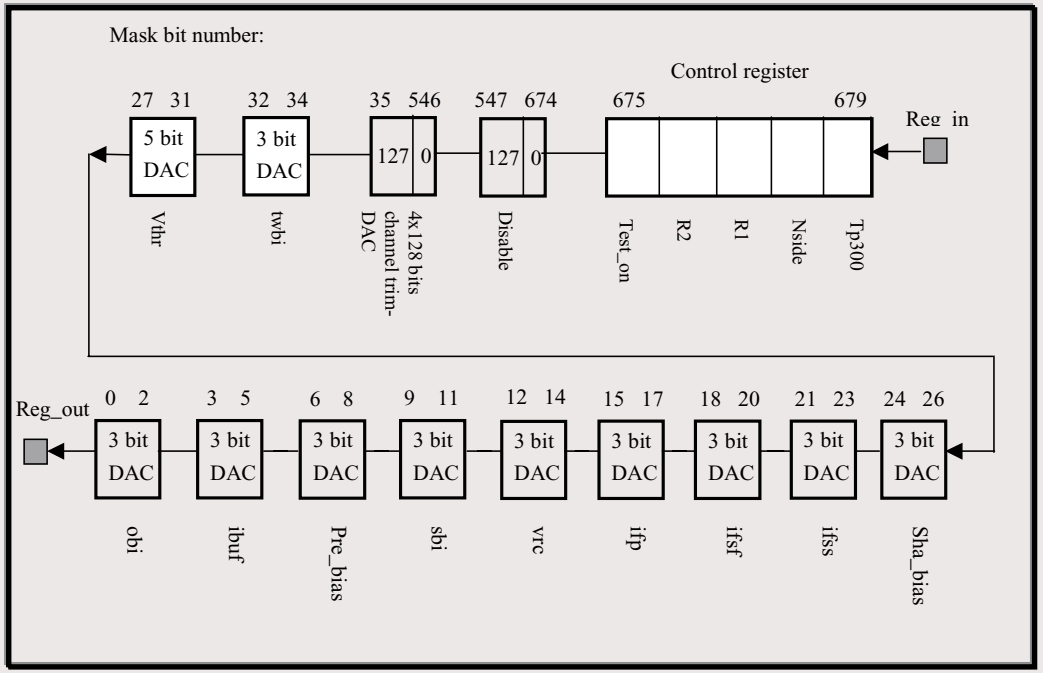
Basic readout unit:

- 512 channels (4 chips)
- parallel readout of all chips



VA1TA schematics





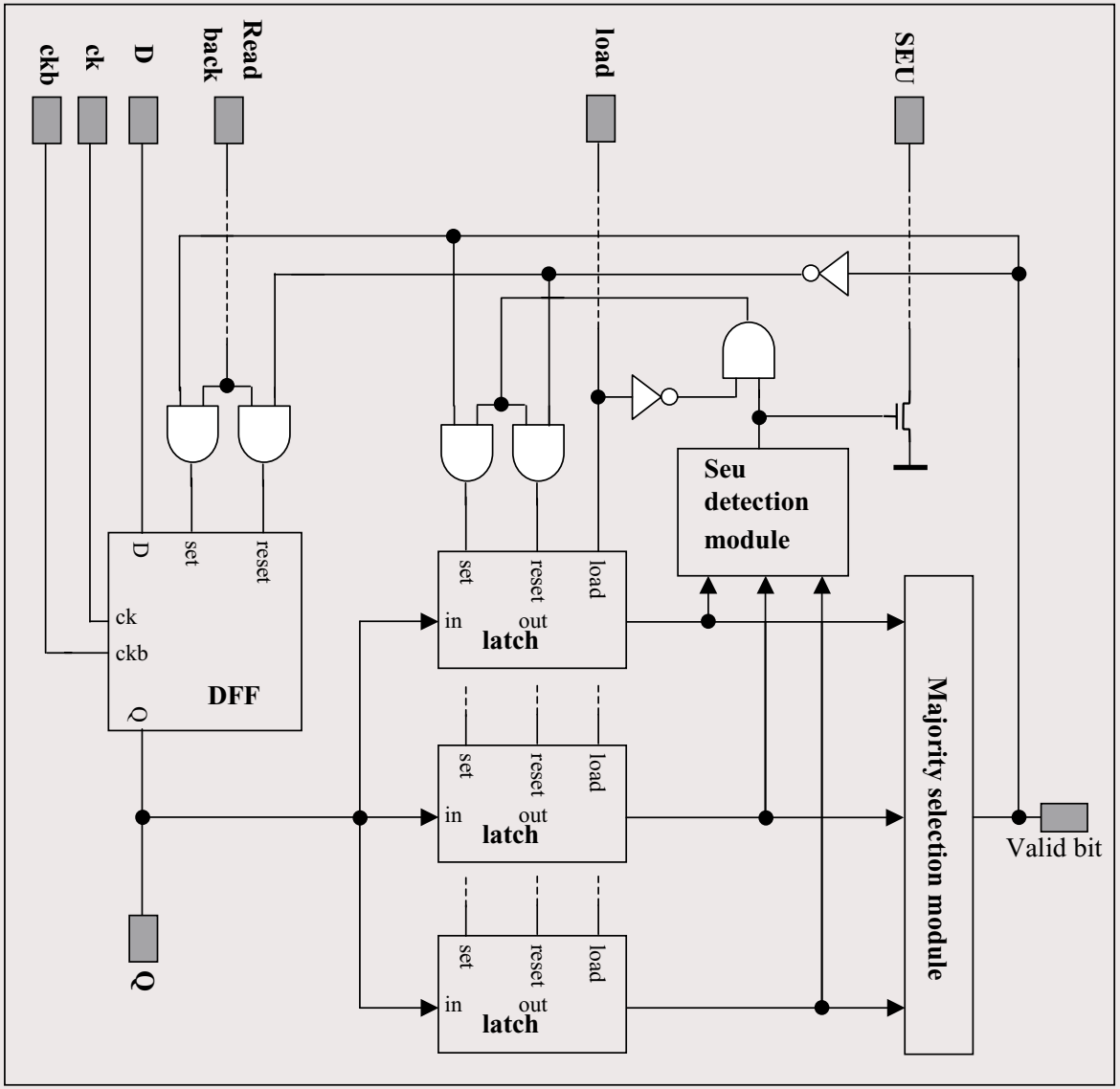
SEU vulnerable parts:

- shift register for analog multiplexer (128 bit)
- shift register for chip control (680 bit)

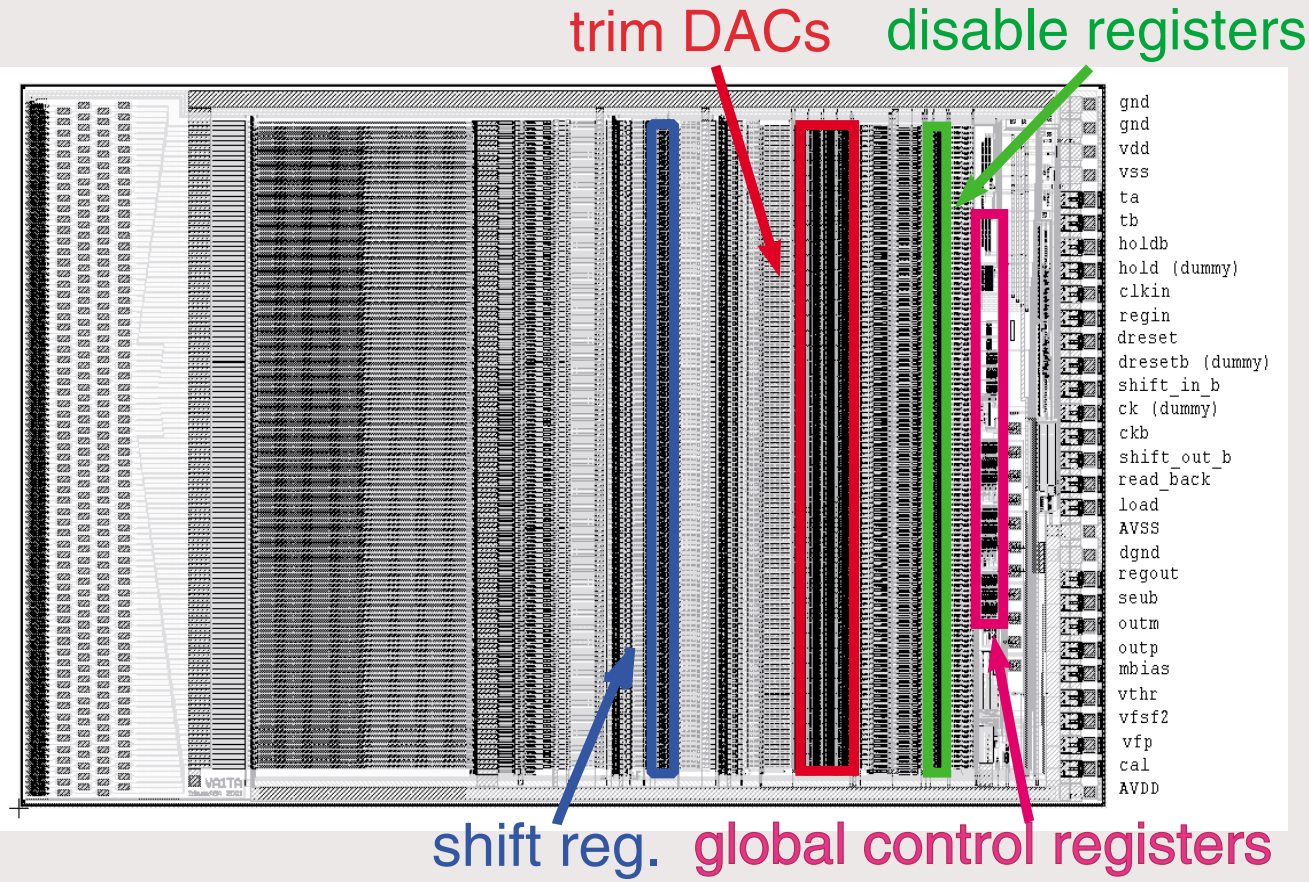
VA1TA SEU detection and correction

Schematics of SEU correction circuit.

- shift register
- three parallel latches
- majority logic for valid bit
- SEU detection and correction



VA1TA SEU sensitive areas



Experimental apparatus

Requirements:

- every day availability
- testing of selective area

The method of testing the SEU with laser pulses has been chosen.

Requirements for the laser:

- short pulses (less than $\approx 100ps$)
- high energy deposited in active the volume per pulse ($\approx 1pJ$)
- small beam size

Laser beam characteristics

Gaussian beam focusing:

- beam size spreading

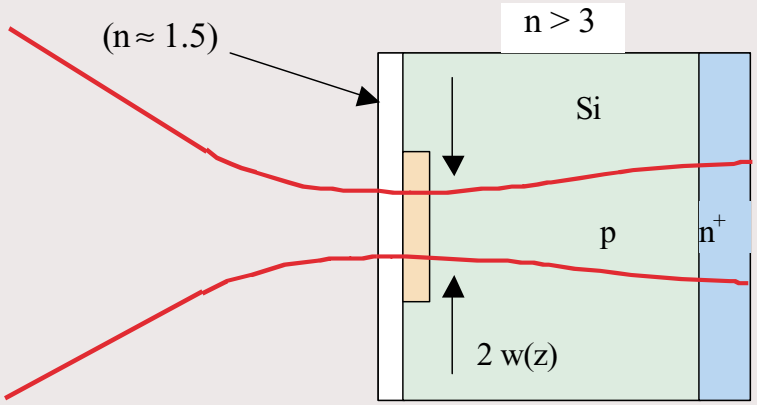
$$w(z) = w_0\sqrt{1+\left(\frac{\lambda z}{\pi w_0^2 n}\right)^2}$$

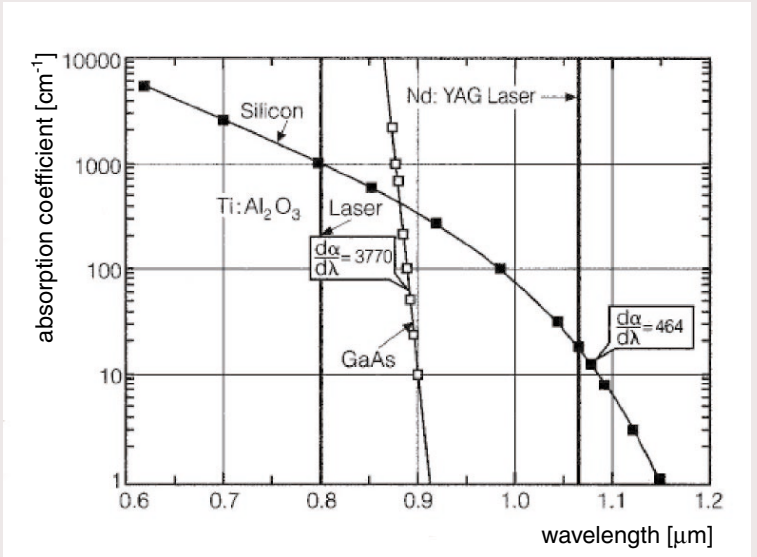
- focus spot size ($w_0 = 2\sigma$)

$$w_0 = \frac{2\lambda f}{\pi D}$$

- depth of focus - Rayleigh range $w(z_R) = \sqrt{2}w_0$

$$z_R = \frac{\pi n w_0^2}{\lambda}$$





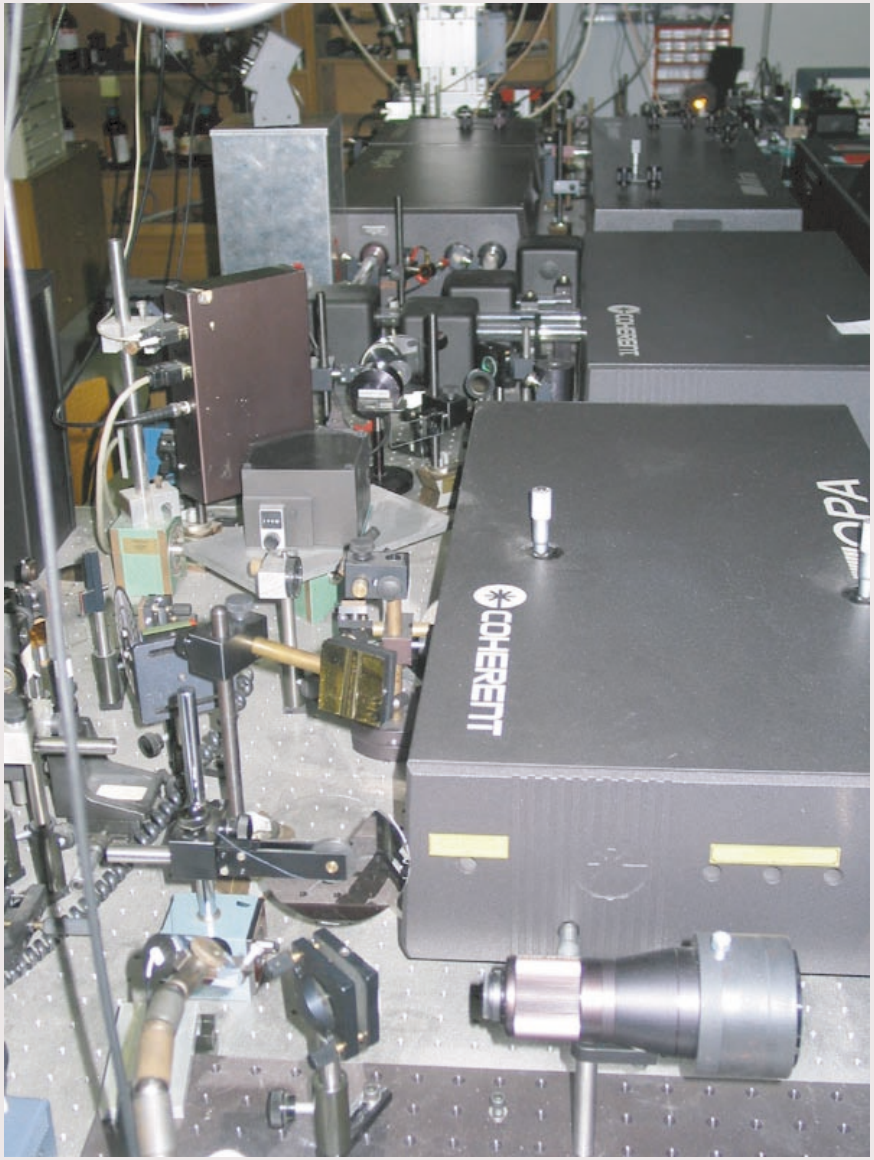
Laser setup 1

- ✦ Ti:Al_2O_3 laser in pulse mode with repetition rate of 250kHz or 125kHz

$$\lambda \approx 800nm$$

$$\Delta t \approx 80fs$$

- ✦ fixed $10^{1.5}$ attenuator
- ✦ variable 1-1000 attenuator
- ✦ focusing and scanning



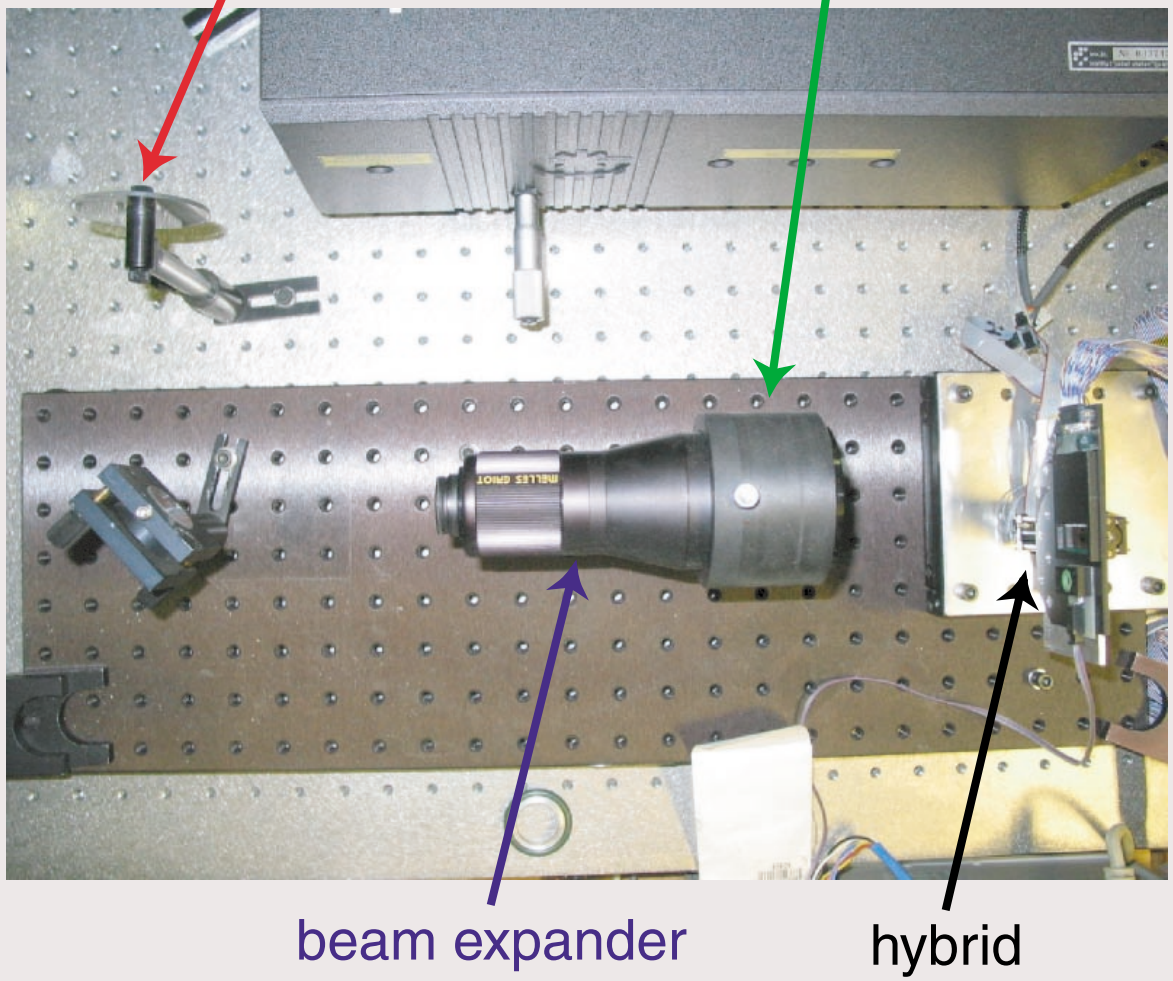
Laser setup 2

- beam expander (Melles Griot 06 GBF 001)
- focusing lens (Melles Griot 06 GLR 001)

$$D = 48mm$$

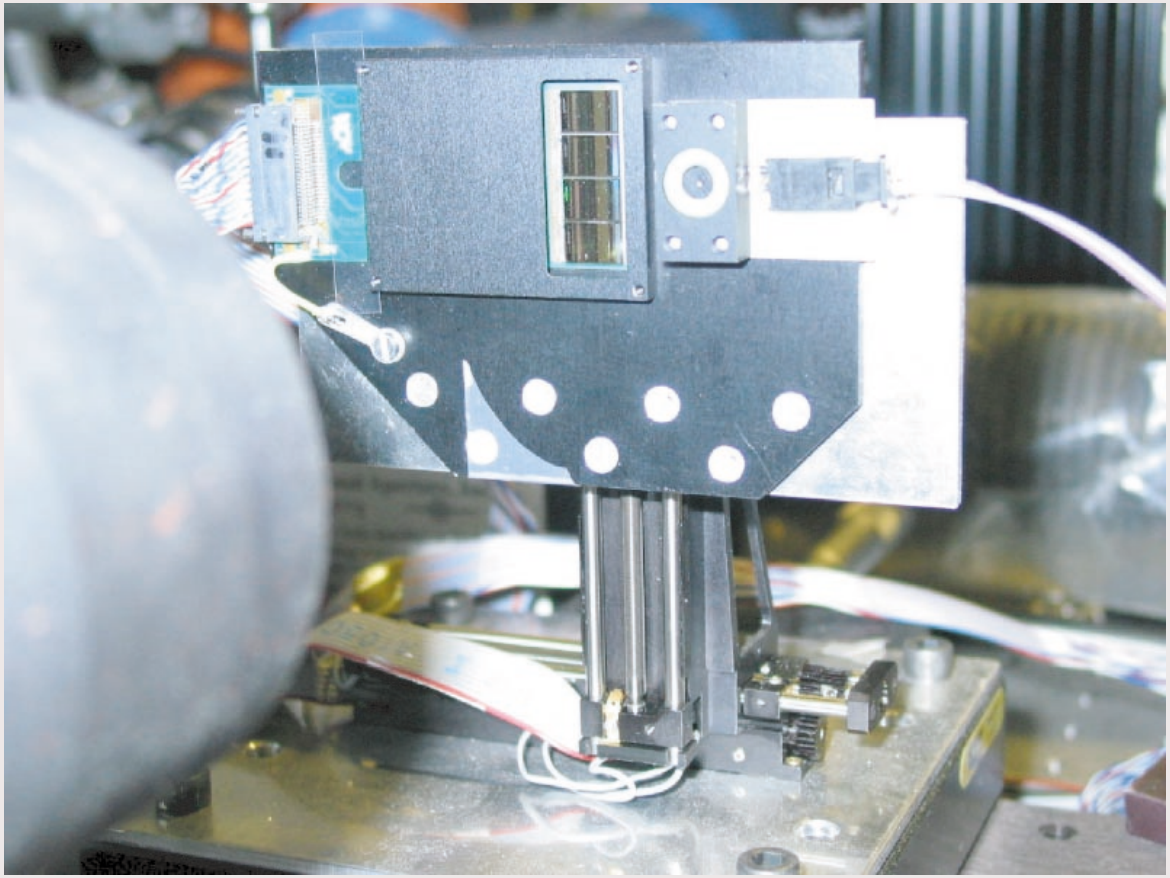
$$f = 120mm$$

- 2+1 D table with hybrid and photo-diode



Hybrid mounting - 2+1 D

- 2D steering table (x,y)
- 1D manual linear stage
- hybrid
- photo-diode with $100\mu m$ diameter aperture



Readout

For readout and biasing a VADAQ system with minor modifications is used (IDEAS)

- computer controlled via parallel port
- provides and monitors all supply and bias currents
- control and readout of the VA1TA chips
- used also for photo-diode current measurement

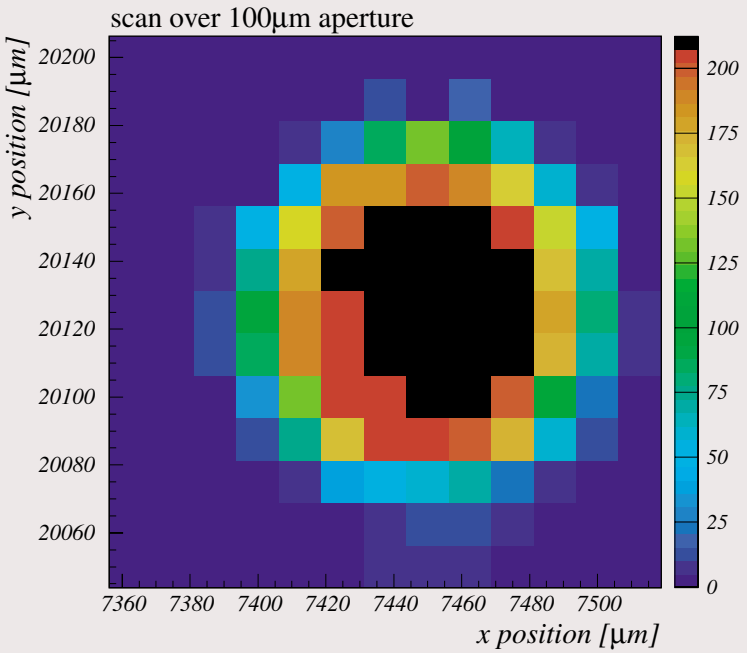
Monitored parameters:

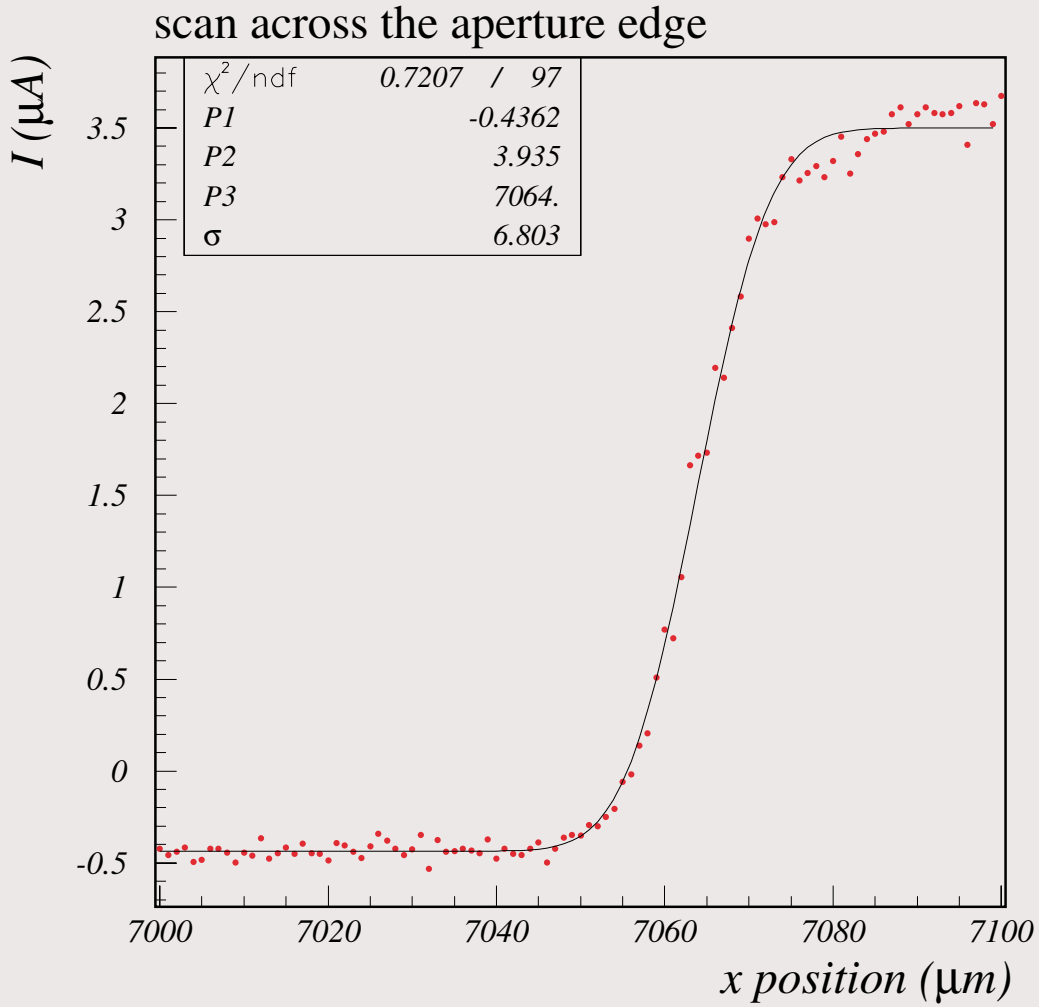
- all bias and supply currents and voltages
- shift register for analog multiplexer
- 8 bit SEU signal counter (255 = overflow)
- shift register for chip control
- state of the valid bits
- photo-diode current

Focus and spot size

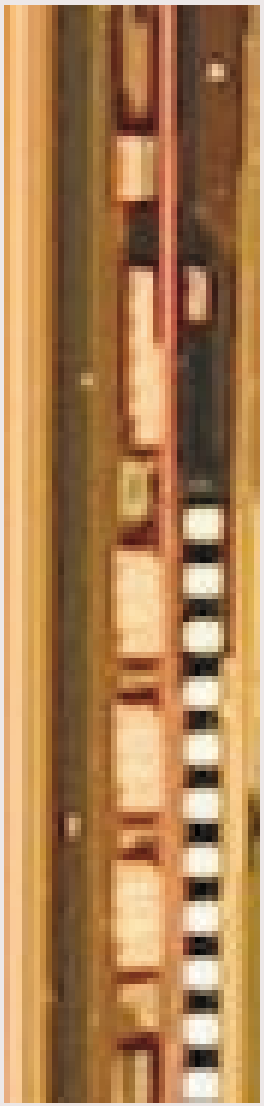
Determination of the focus position and spot size by scanning over the photo-diode with $100\mu m$ diameter aperture.

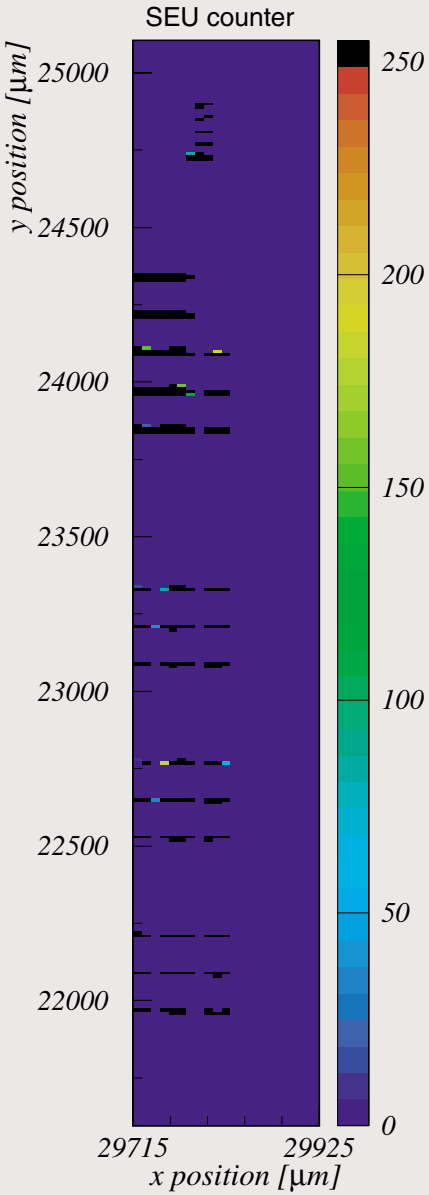
- $\sigma \approx 7\mu m$ $\longrightarrow$

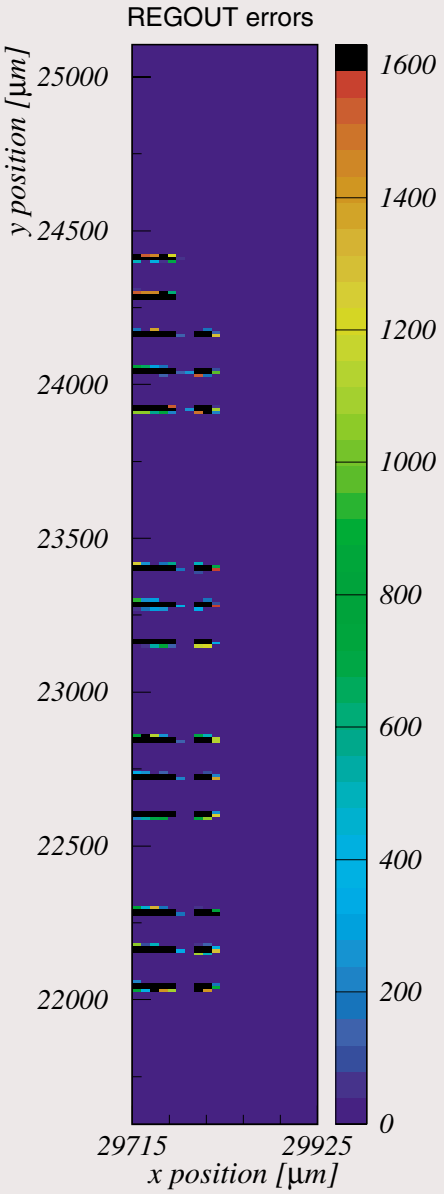




Global registers







TA disable and global registers

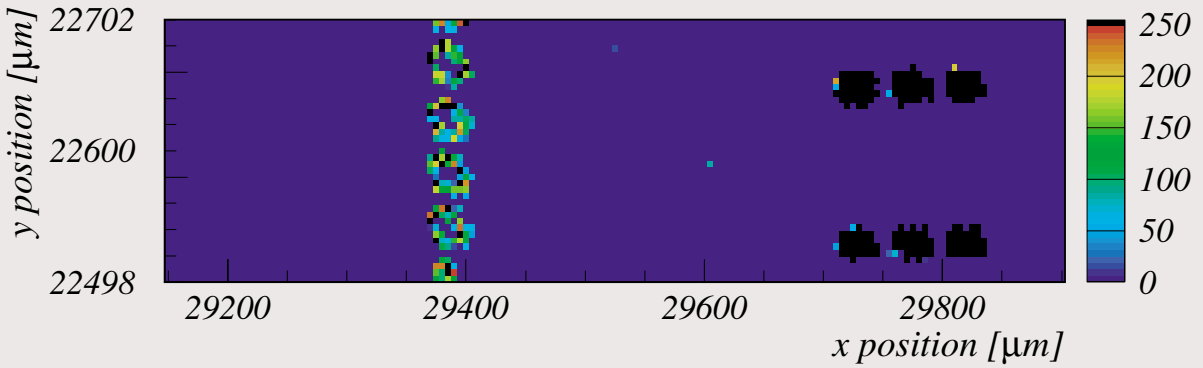
Test sequence:

- move to position
- reset SEU counter
- wait for $\approx 0.5s$
- read SEU counter
- clock out the chip control register and count the number of flipped bits

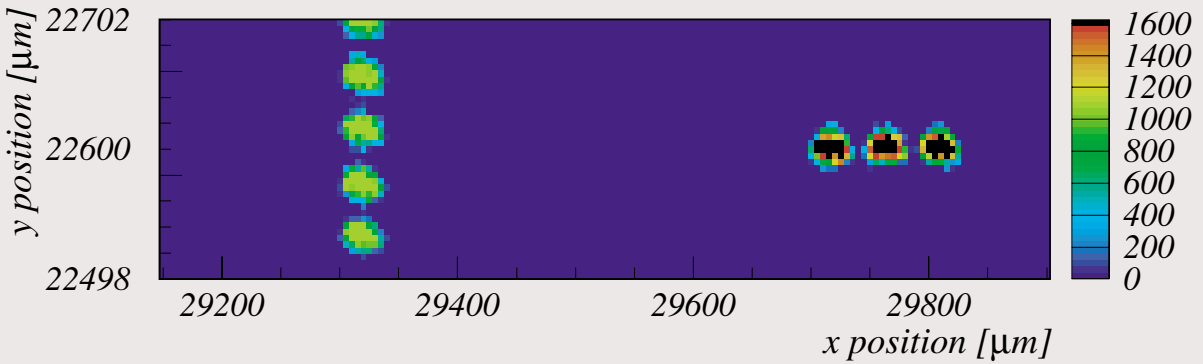
- all the 0's in the shift register for chip control (REGOUT) that pass the laser point are flipped to 1

$$0 \rightarrow 1$$

- SEU counter



- REGOUT errors

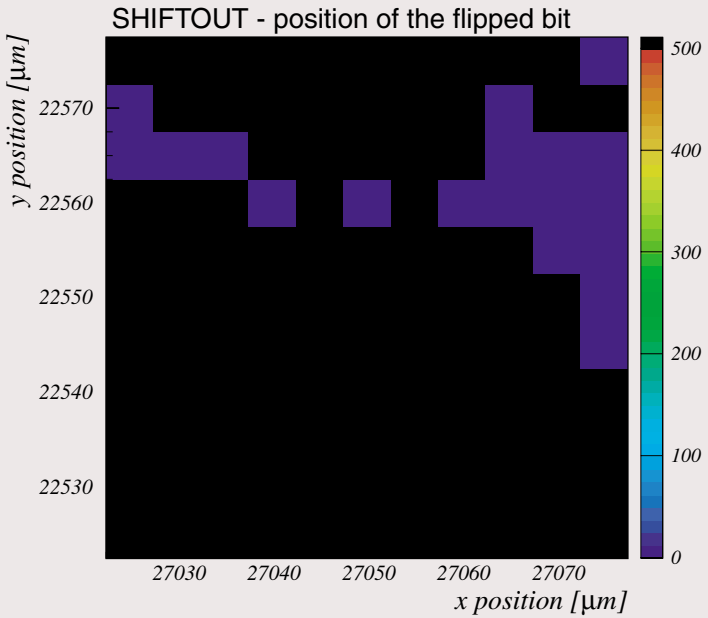


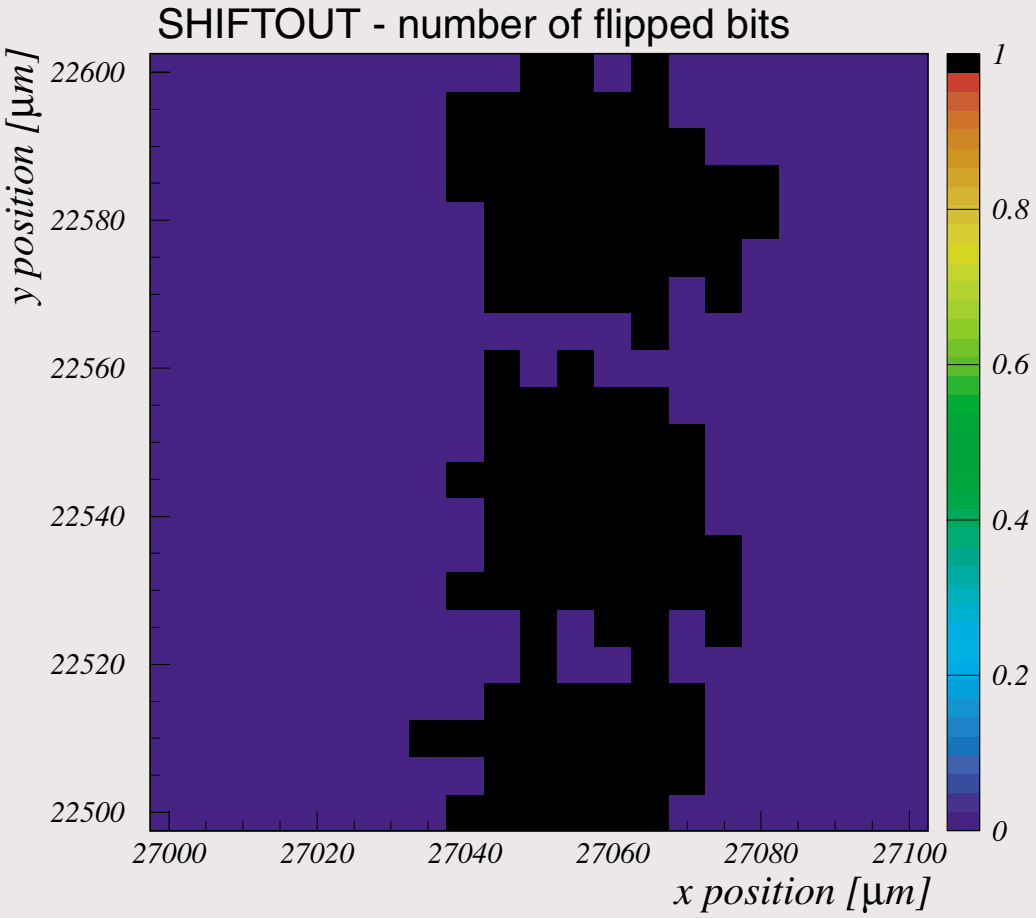
SHIFTOUT errors

Test sequence:

- move to position
- reset of shift register (all bits 1)
- clock one bit (0) thru the register and count the number of flipped bits
- 0 bit flipped to 1

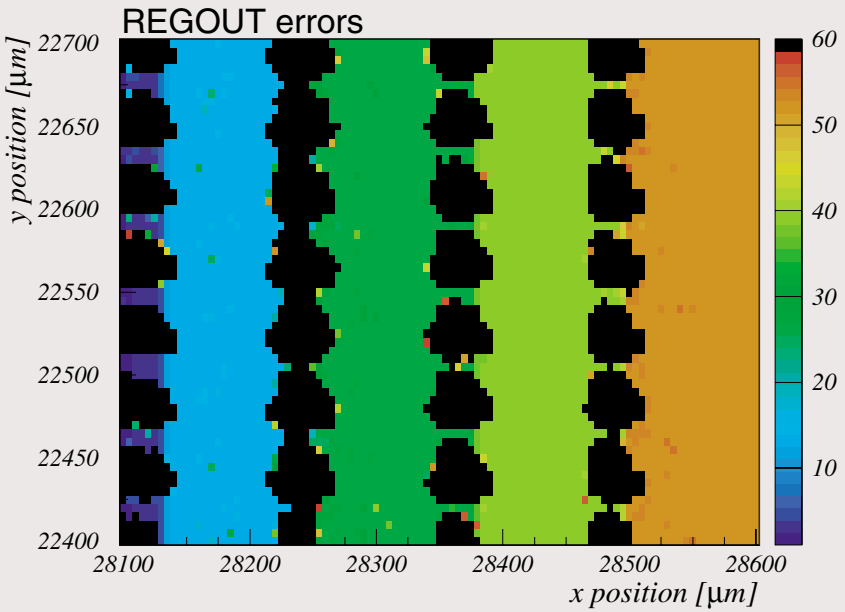
$0 \rightarrow 1$

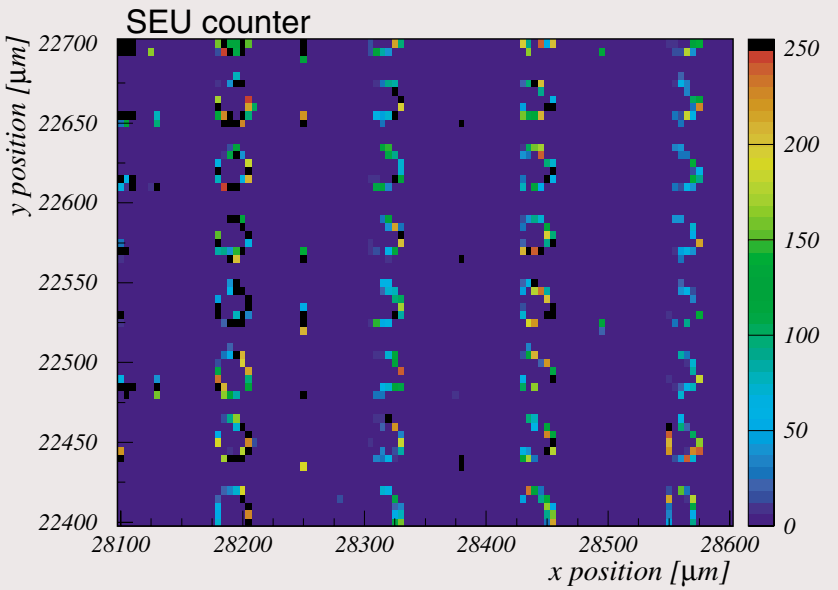


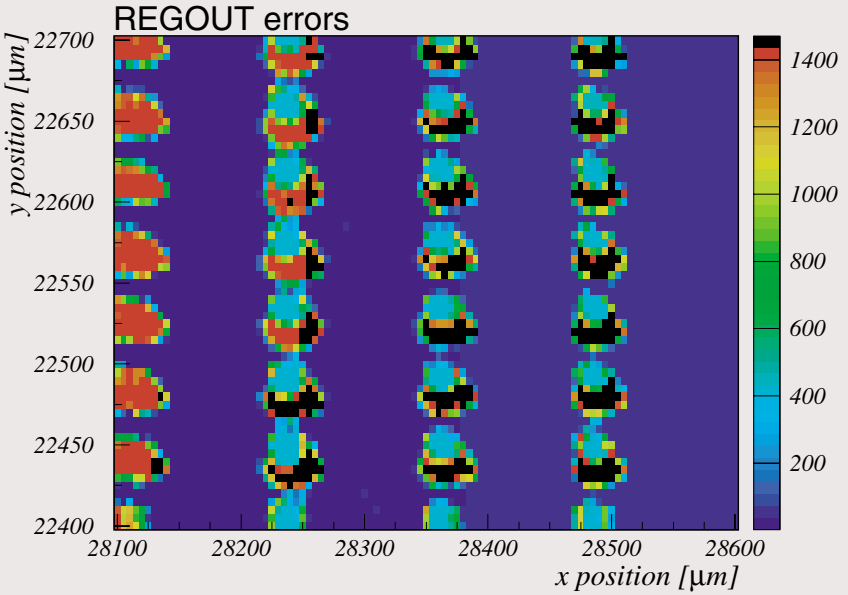


Trim DACs

- scan over the trim DACs area with higher pulse energy
- permanent change in chip control register observed

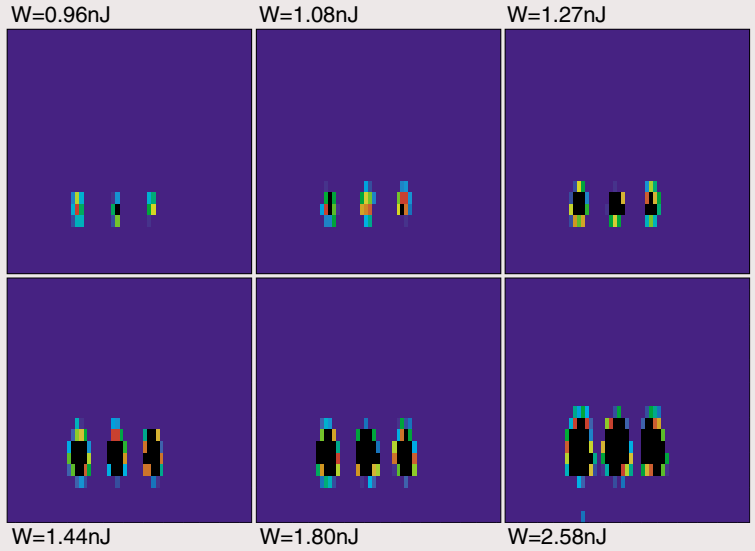


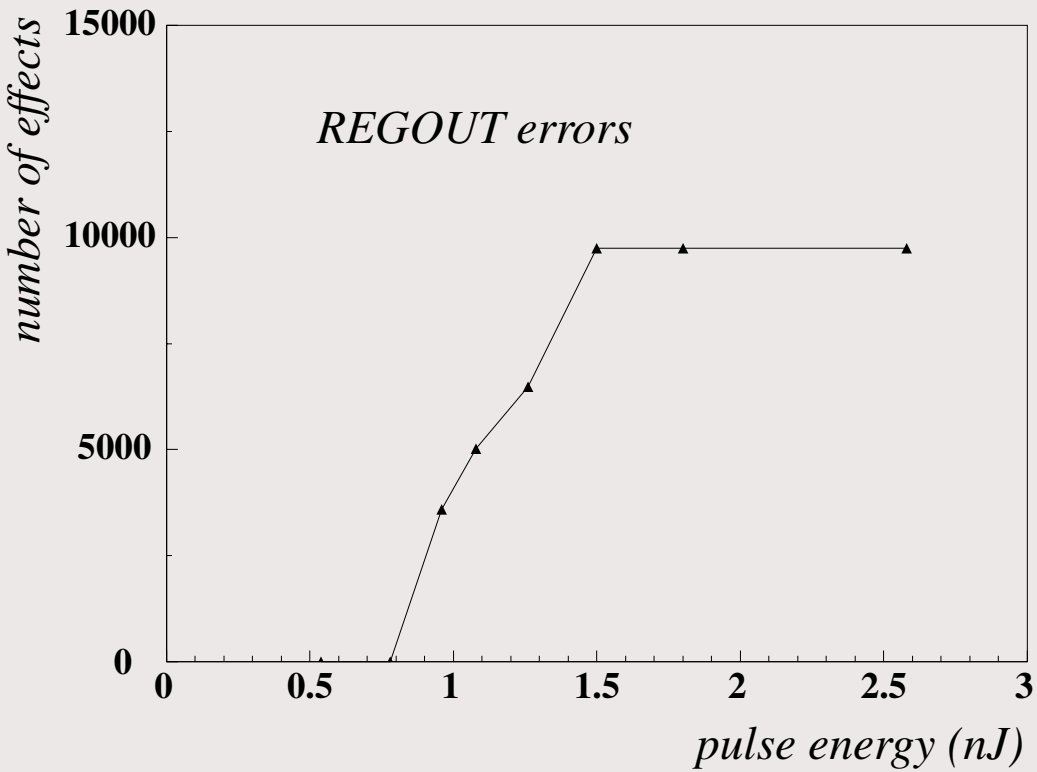




SEU threshold - REGOUT errors

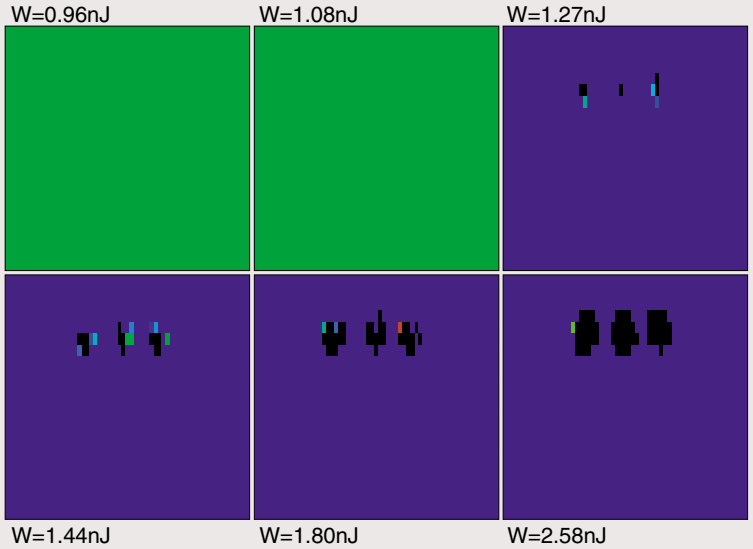
- number of the REGOUT errors as a function of the pulse energy

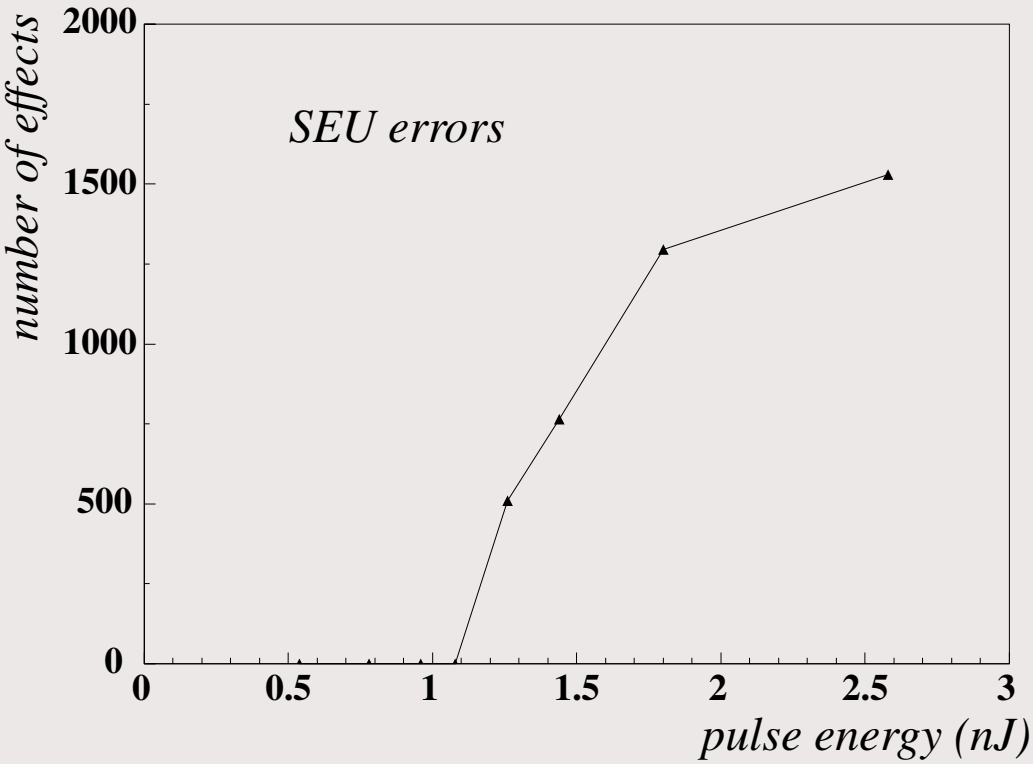




SEU threshold - SEU counter

- number of the SEU pulses as a function of the pulse energy





Summary and plans

- Setup for the SEU testing with laser has been constructed and is now being routinely used
- potential SEU sensitive spots were identified and compared with the chip layout

Next steps:

- go to a smaller spot size (using an additional beam expander)
- clarify open questions (permanent chip control register change)