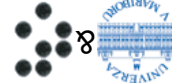


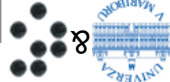
1. Introduction - reminder
2. Target regions
3. Measurements
4. Summary and plans

**Samo Korpar**  
University of Maribor and J. Stefan Institute  
November 21, 2002  
SVD meeting

## SEU STUDIES, UPDATE

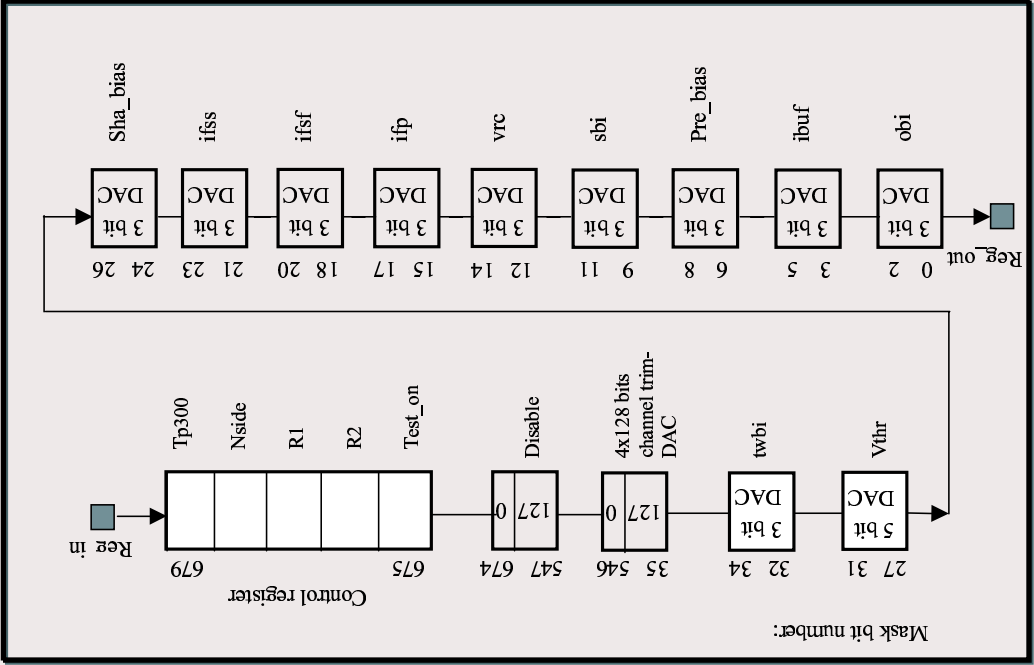
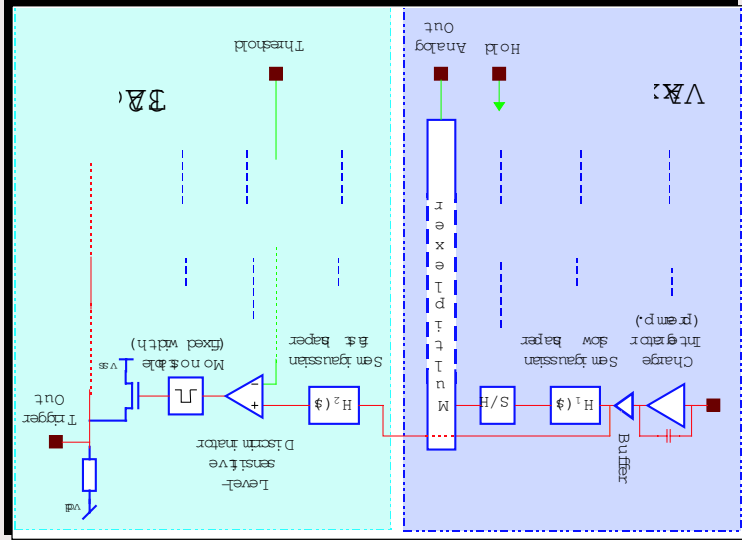


# VA1TA schematics



SEU vulnerable parts:

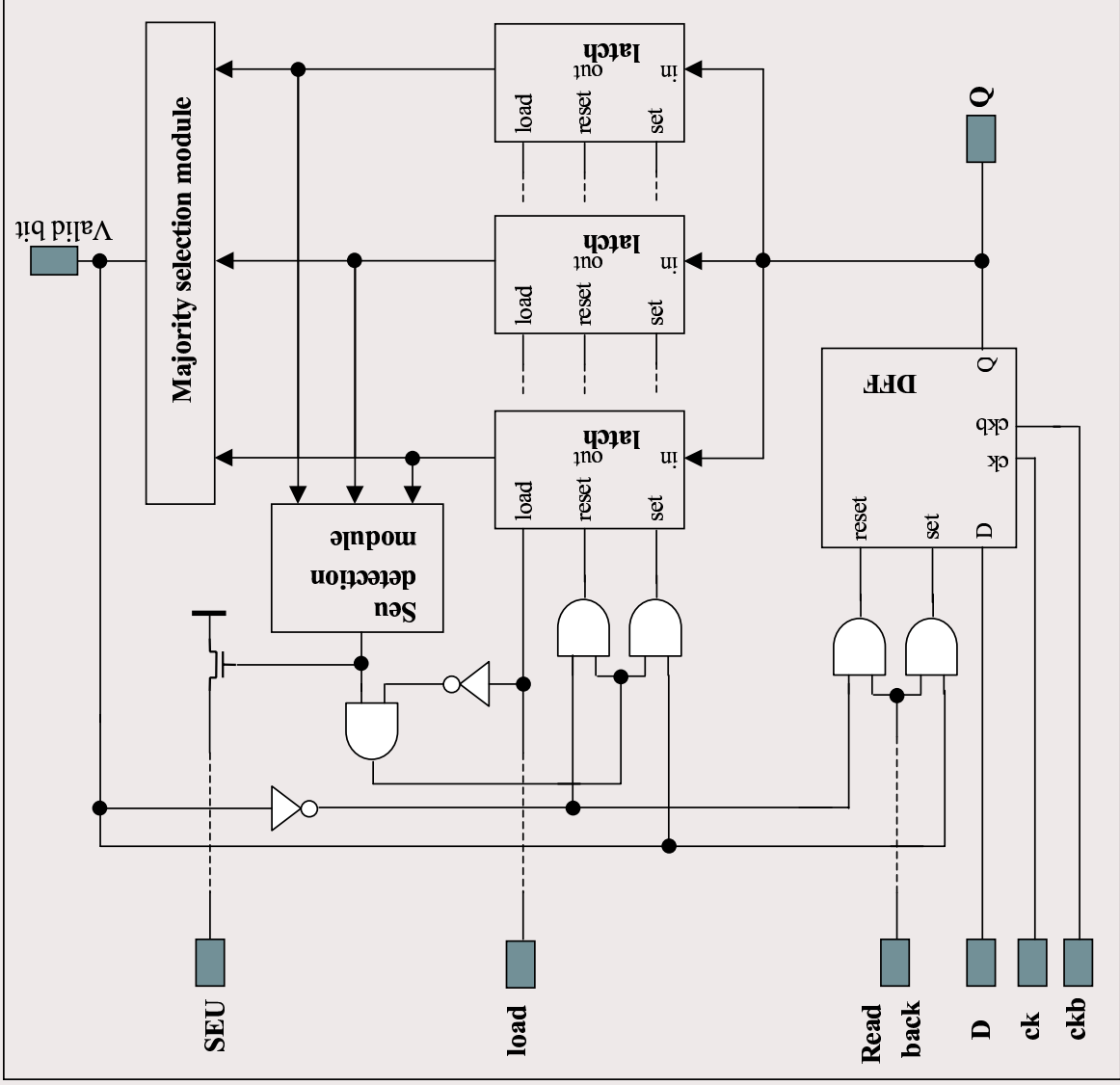
- ◆ shift register for analog multiplexer (128 bit)
- ◆ shift register for chip control (680 bit)

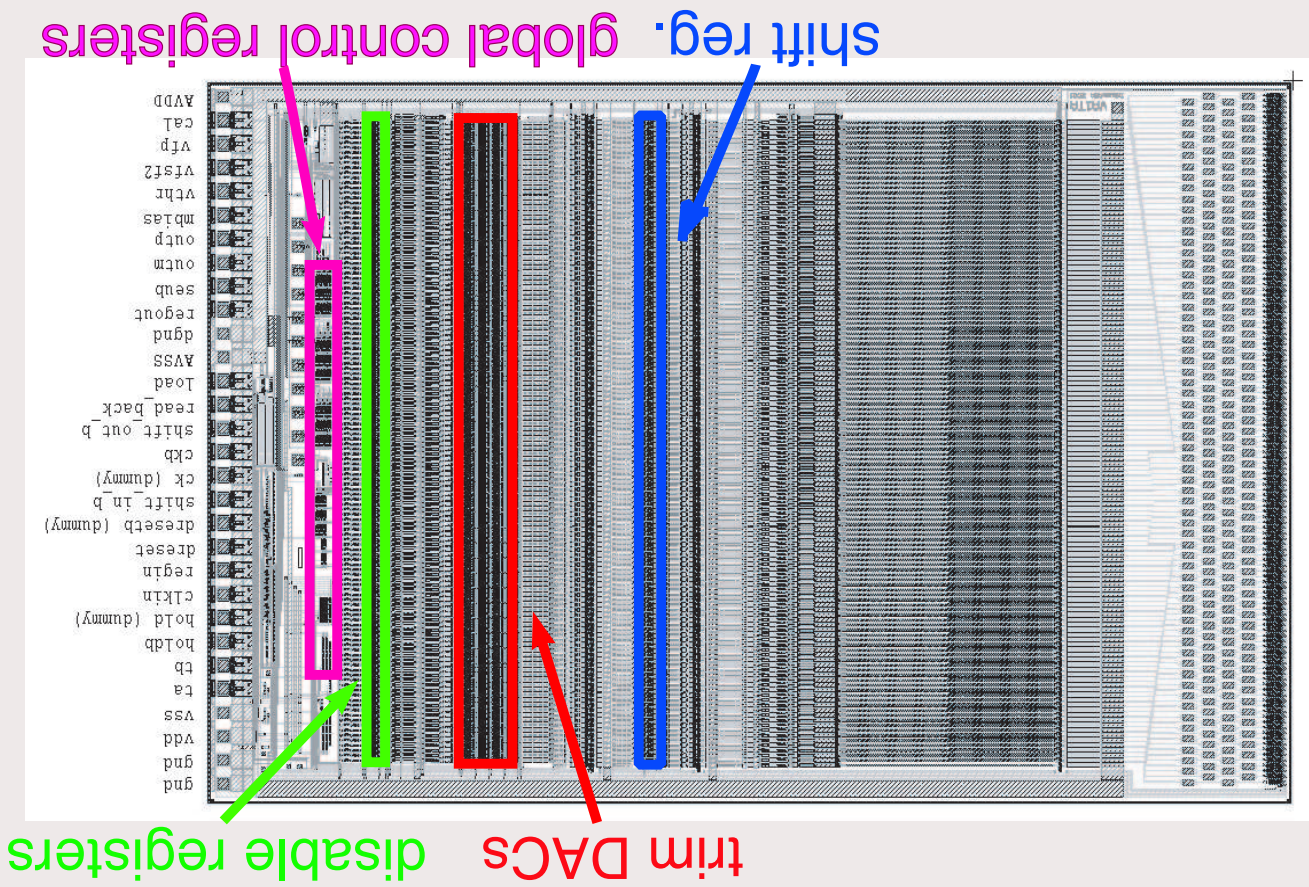


# VAITA SEU detection and correction

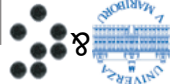
- ◆ shift register
- ◆ three parallel latches
- ◆ majority logic for valid bit
- ◆ SEU detection and correction

Schematics of SEU correction circuit.





VAITA SEU sensitive areas



# Laser beam characteristics

Requirements for the laser:

- ◆ short pulses (less than  $\approx 100ps$ )
- ◆ high energy deposited in active the volume per pulse ( $\approx 1pJ$ )
- ◆ small beam size

Gaussian beam focusing:

- ◆ beam size spreading

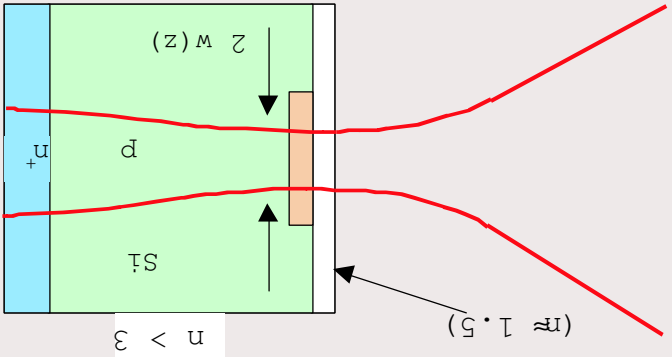
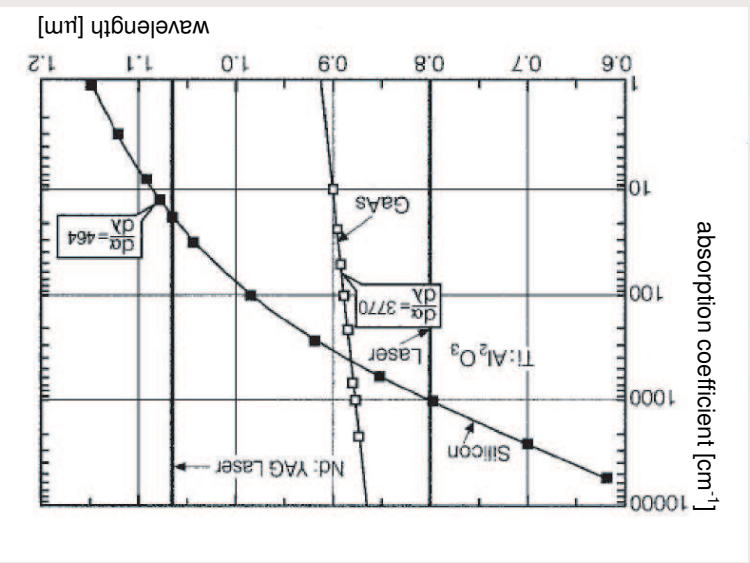
$$w(z) = w_0 \sqrt{1 + \left(\frac{\lambda z}{\pi w_0^2 n}\right)^2}$$

- ◆ focus spot size ( $w_0 = 2\sigma$ )

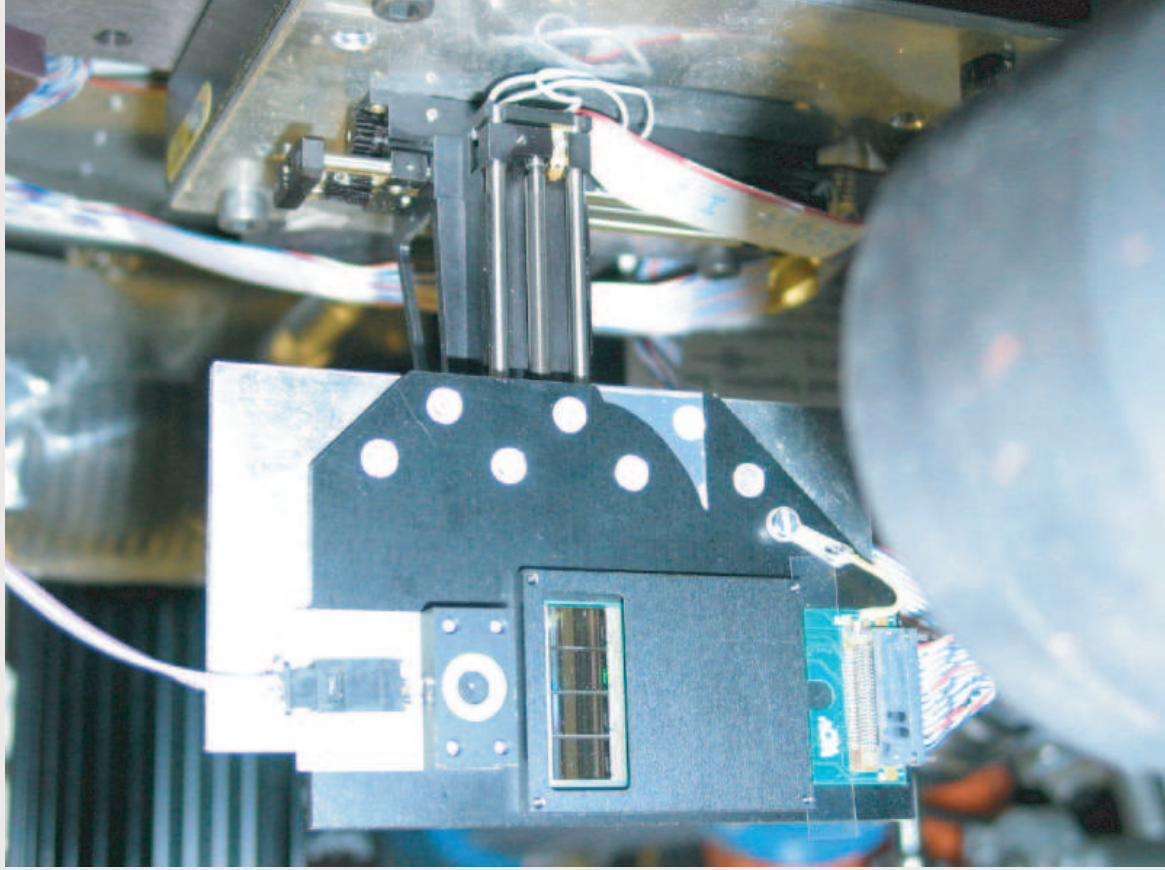
$$w_0 = \frac{2\lambda f}{\pi D}$$

- ◆ depth of focus - Rayleigh range  $w(z_R) = \sqrt{2}w_0$

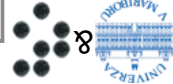
$$z_R = \frac{\lambda}{\pi n w_0^2}$$



- ◆ 2D steering table (x,y)
- ◆ 1D manual linear stage
- ◆ hybrid
- ◆ photo-diode with  $100\mu m$  diameter aperture



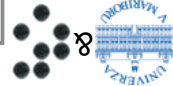
## Hybrid mounting - 2+1 D



## Readout

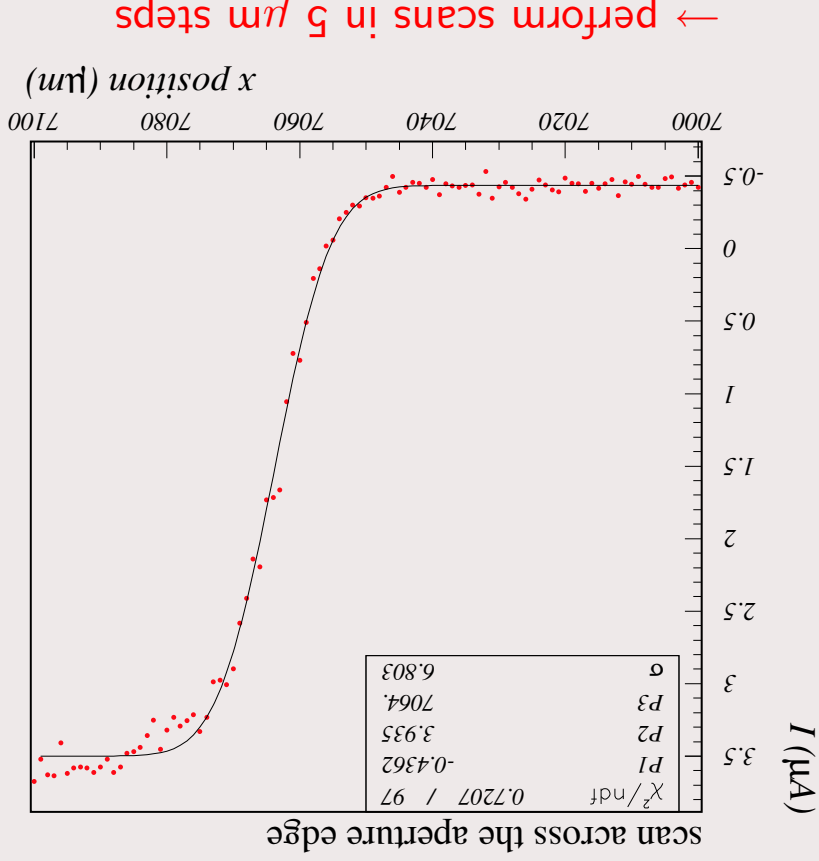
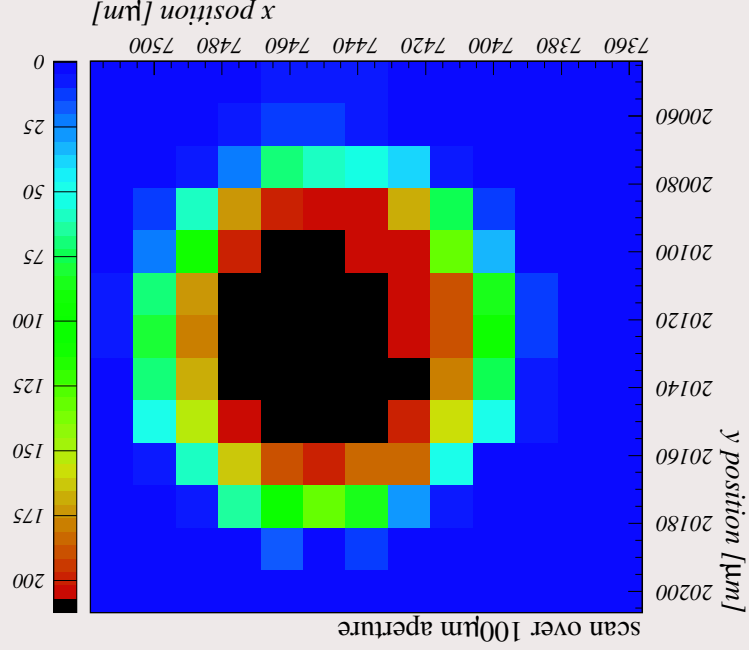
Monitored parameters:

- ◆ all bias and supply currents and voltages
- ◆ shift register for analog multiplexer
- ◆ 8 bit SEU signal counter (255 = overflow)
- ◆ shift register for chip control
- ◆ state of the valid bits
- ◆ photo-diode current



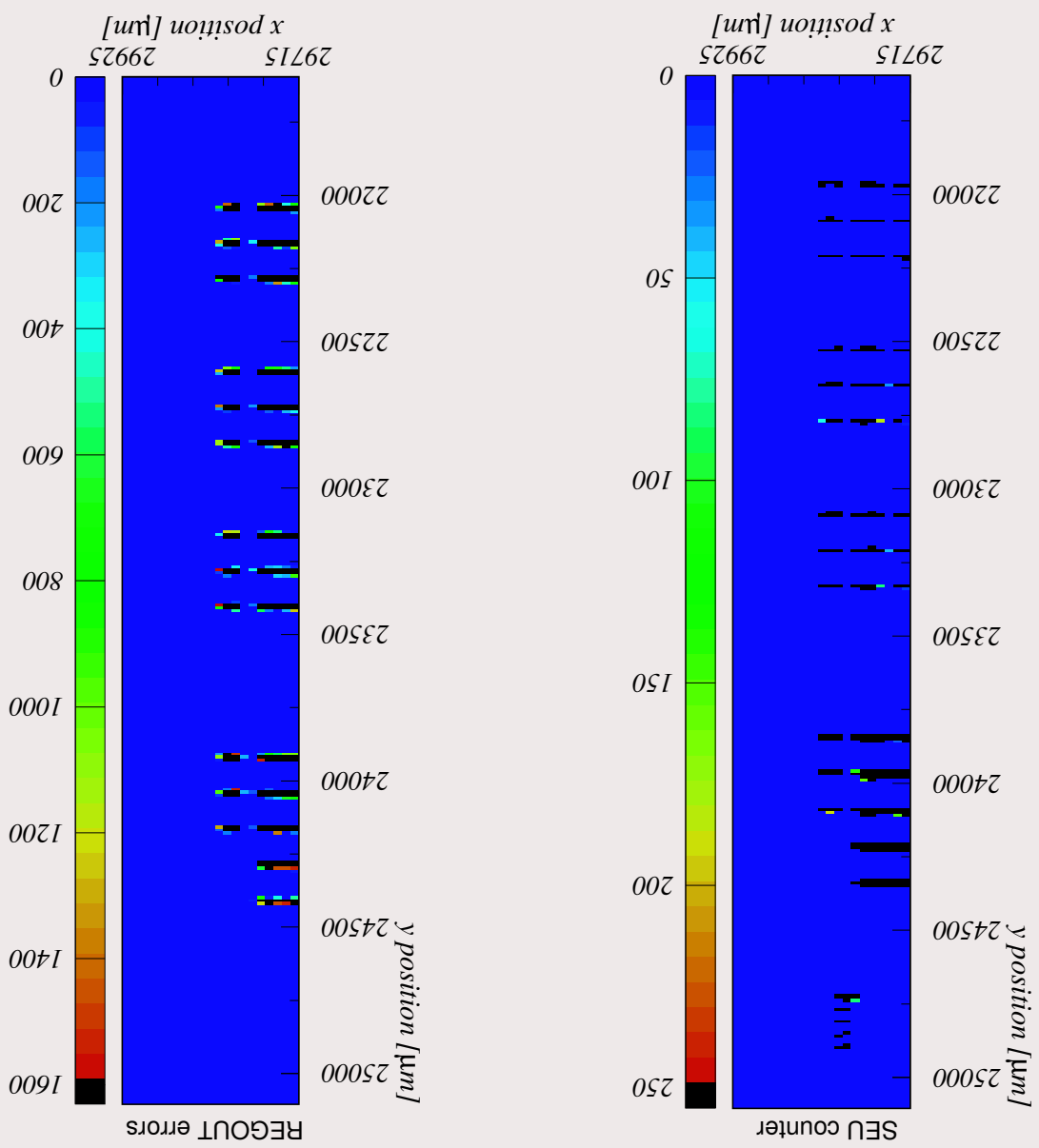
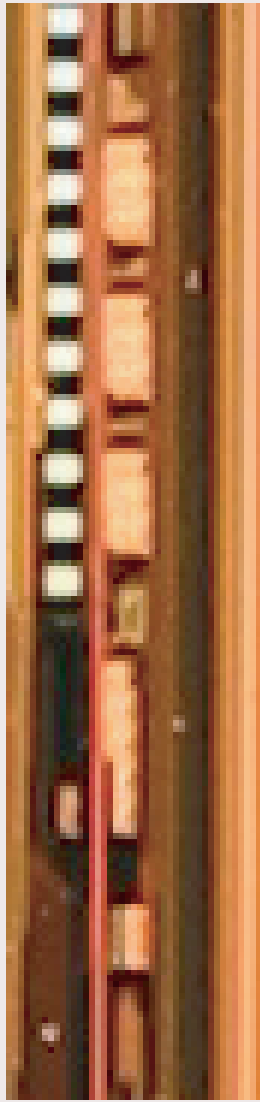
Determination of the focus position and spot size by scanning over the photo-diode with  $100\mu\text{m}$

diameter aperture.  $\sigma \approx 7\mu\text{m}$

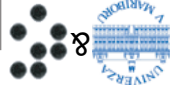


→ perform scans in 5  $\mu\text{m}$  steps





Global registers



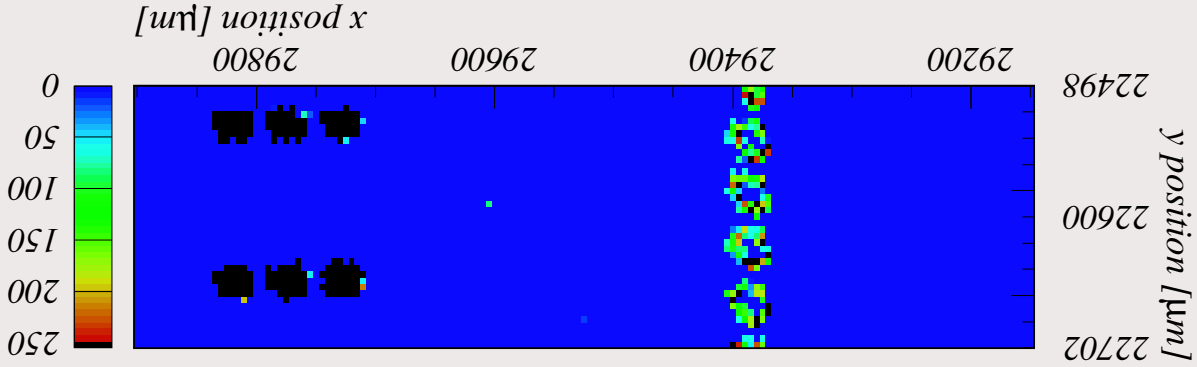
# TA disable and global registers

Test sequence:

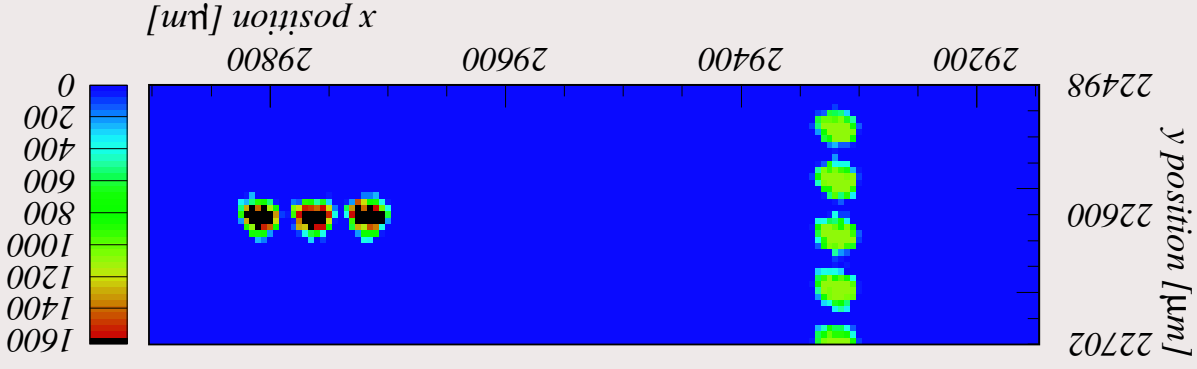
- ◆ move to position
- ◆ reset SEU counter
- ◆ wait for  $\approx 0.5s$
- ◆ read SEU counter
- ◆ clock out the chip control register and count the number of flipped bits

- ◆ all the 0's in the shift register for chip control (REGOUT) that pass the laser point are flipped to 1
- 0  $\leftarrow$  1

◆ SEU counter



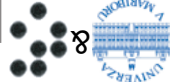
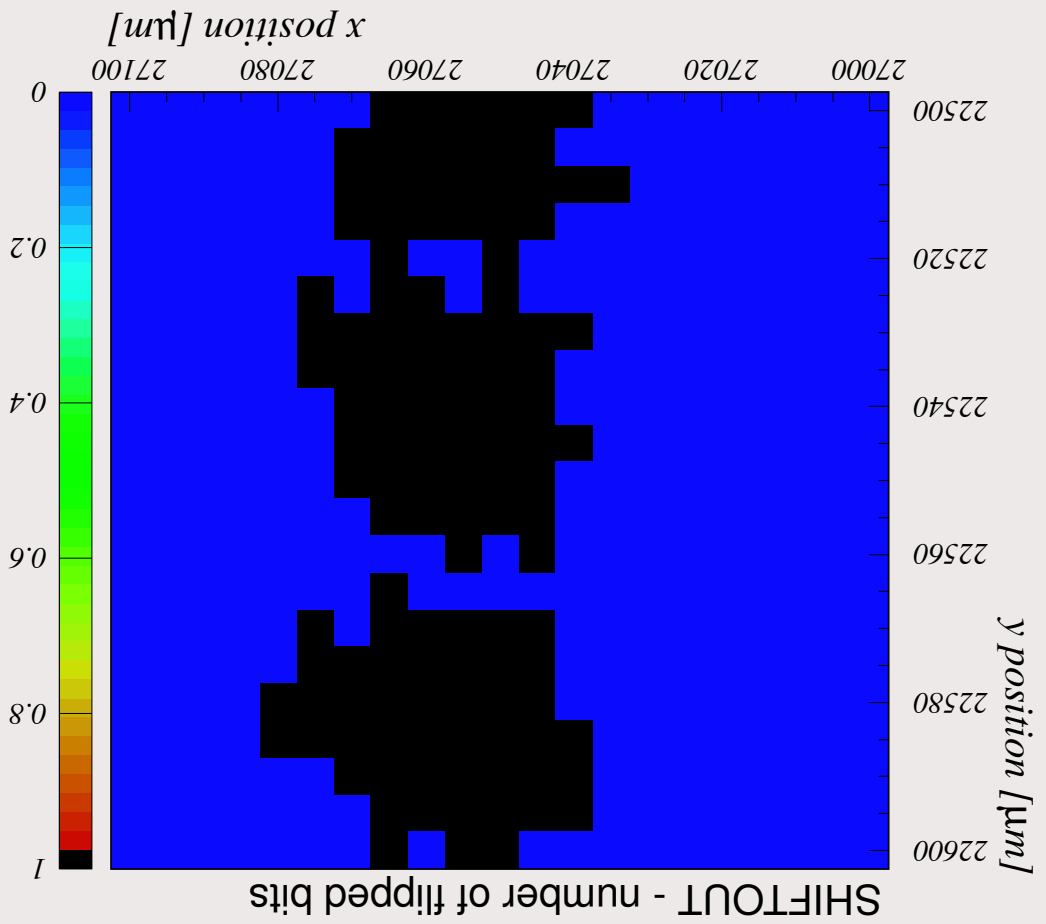
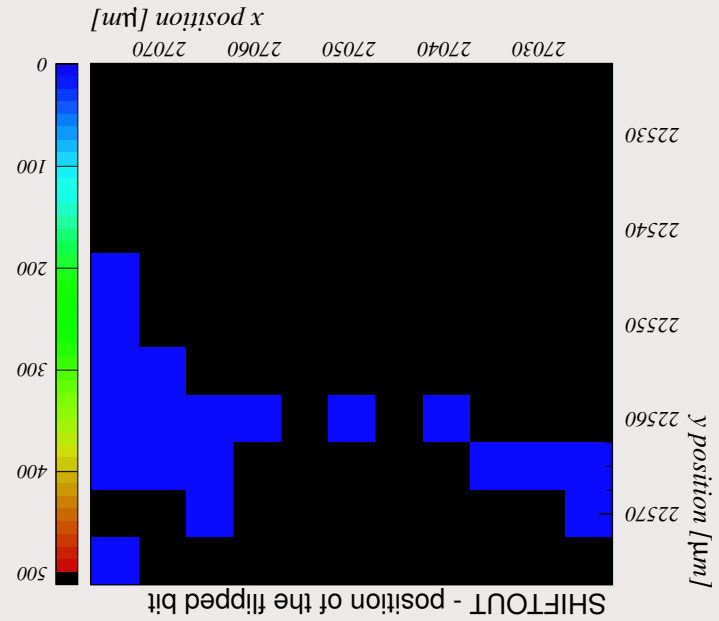
◆ REGOUT errors



# SHIFTOUT errors

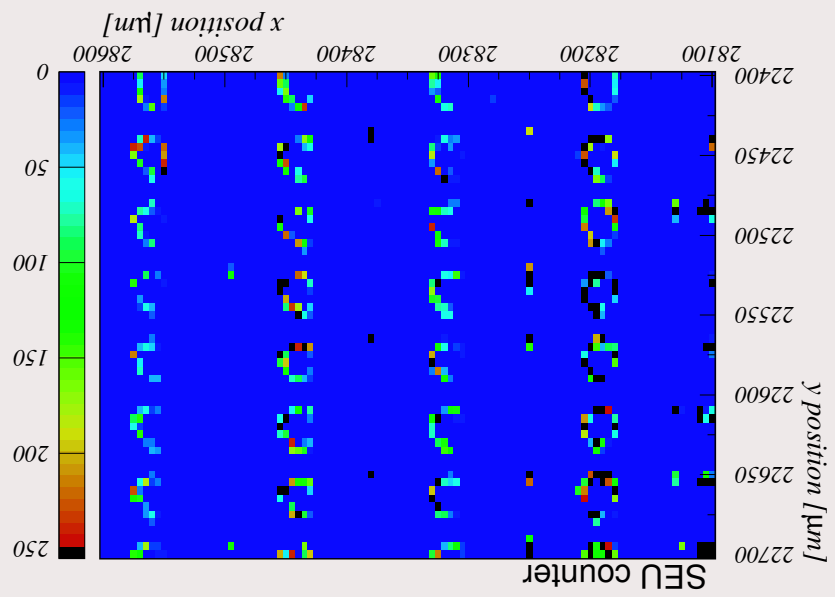
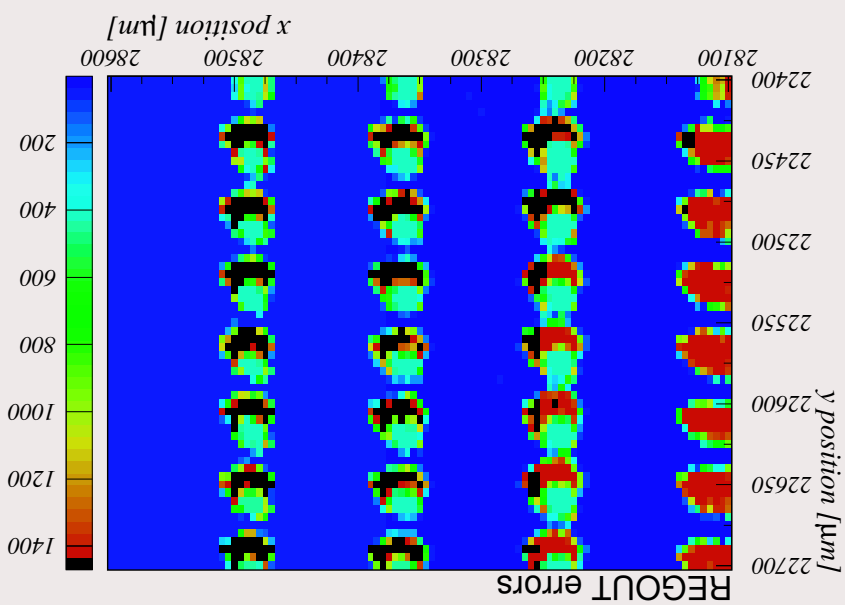
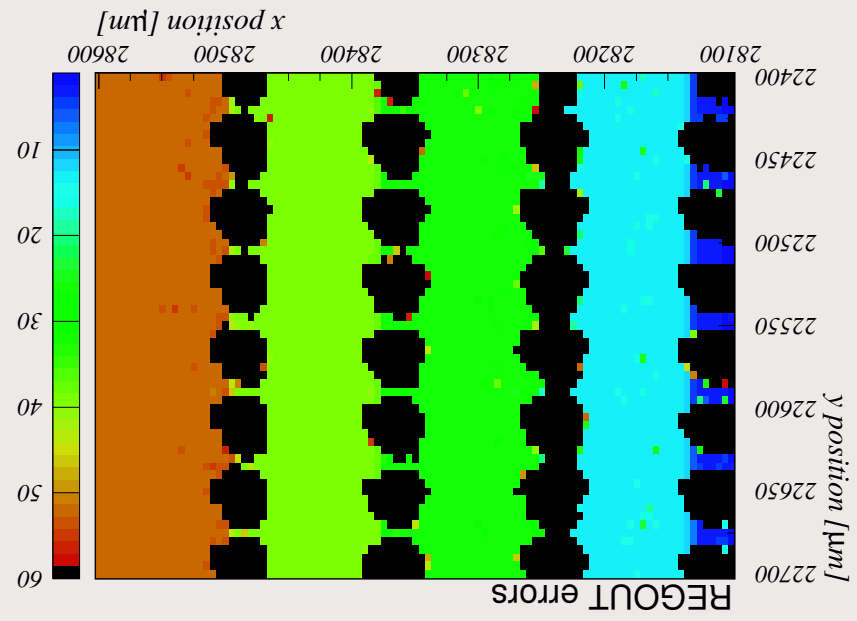
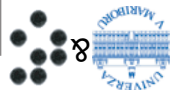
Test sequence:

- ◆ move to position
  - ◆ reset of shift register (all bits 1)
  - ◆ clock one bit (0) thru the register and count the number of flipped bits
  - ◆ 0 bit flipped to 1
- 0 ← 1



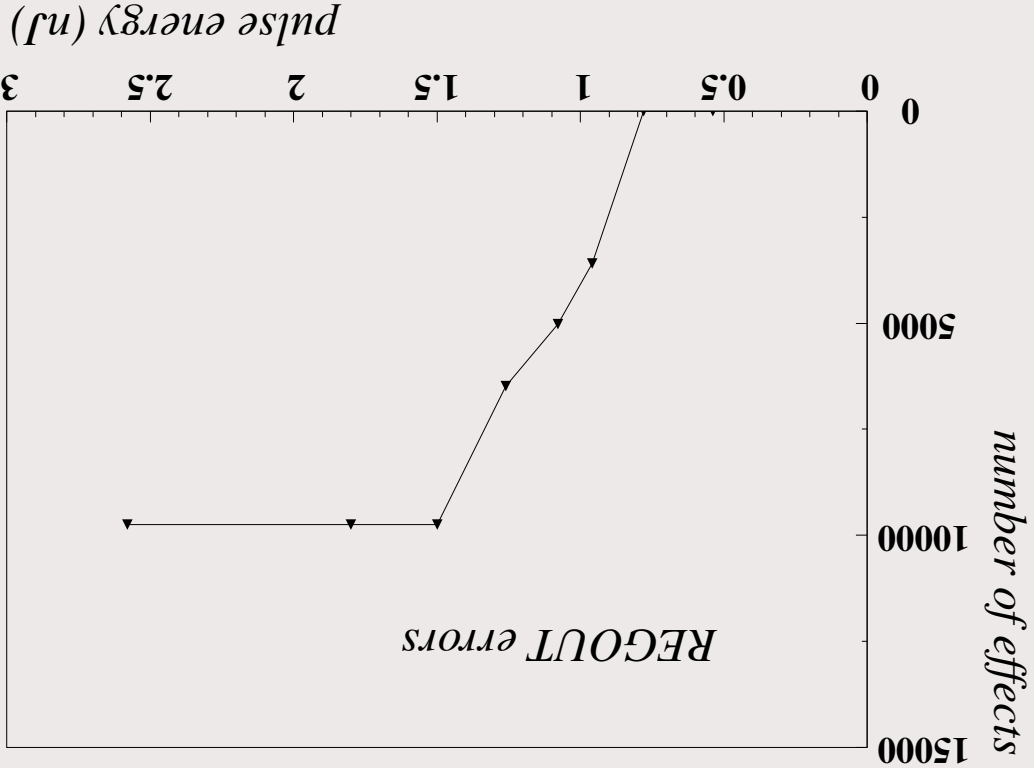
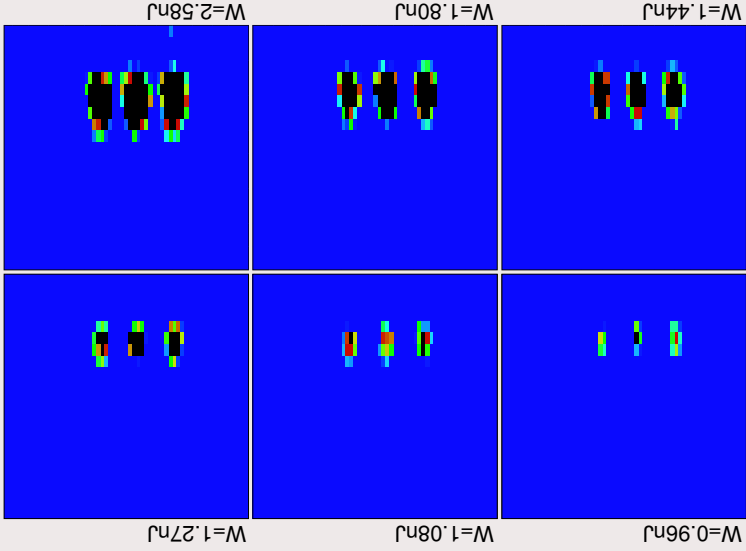
- ◆ scan over the trim DACs area with higher pulse energy
- ◆ permanent change in chip control register observed

### Trim DACs



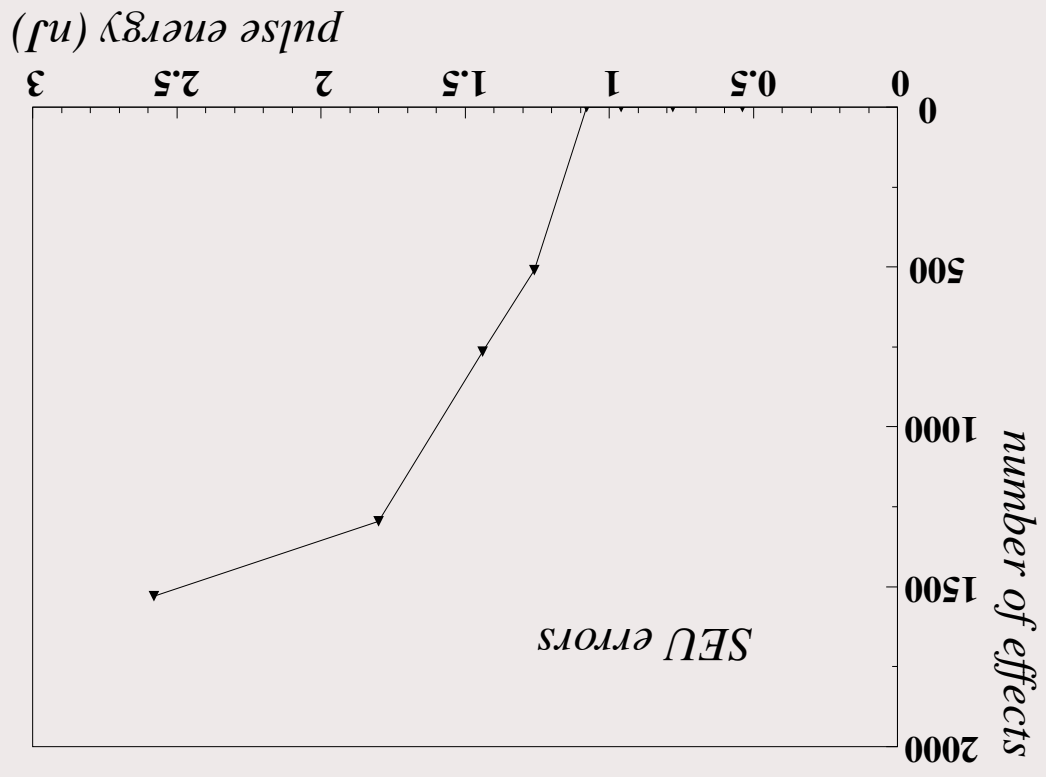
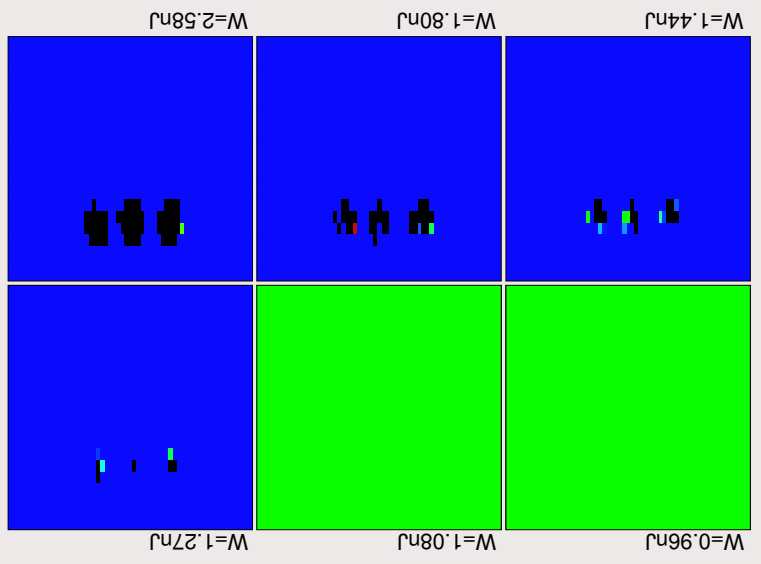
# SEU threshold - REGOUT errors

◆ number of the REGOUT errors as a function of the pulse energy



# SEU threshold - SEU counter

◆ number of the SEU pulses as a function of the pulse energy



- ◆ Setup for the SEU testing with laser has been constructed and is now being routinely used
- ◆ potential SEU sensitive spots were identified and compared with the chip layout

Next steps:

- ◆ get a detailed layout (discussed with IDEAS - Bjorn and Sindre)
- ◆ go to a smaller spot size (using an additional beam expander)
- ◆ clarify open questions (permanent chip control register change)

## Summary and plans

