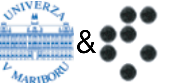

SEU studies, update

Samo Korpar
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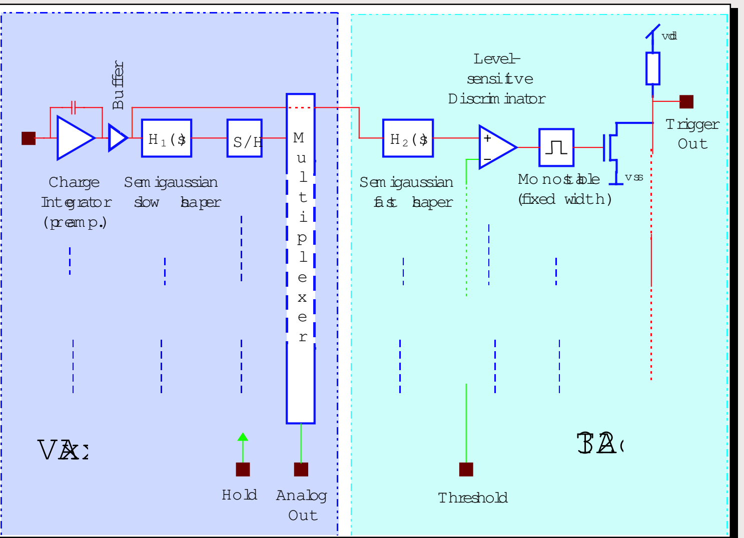
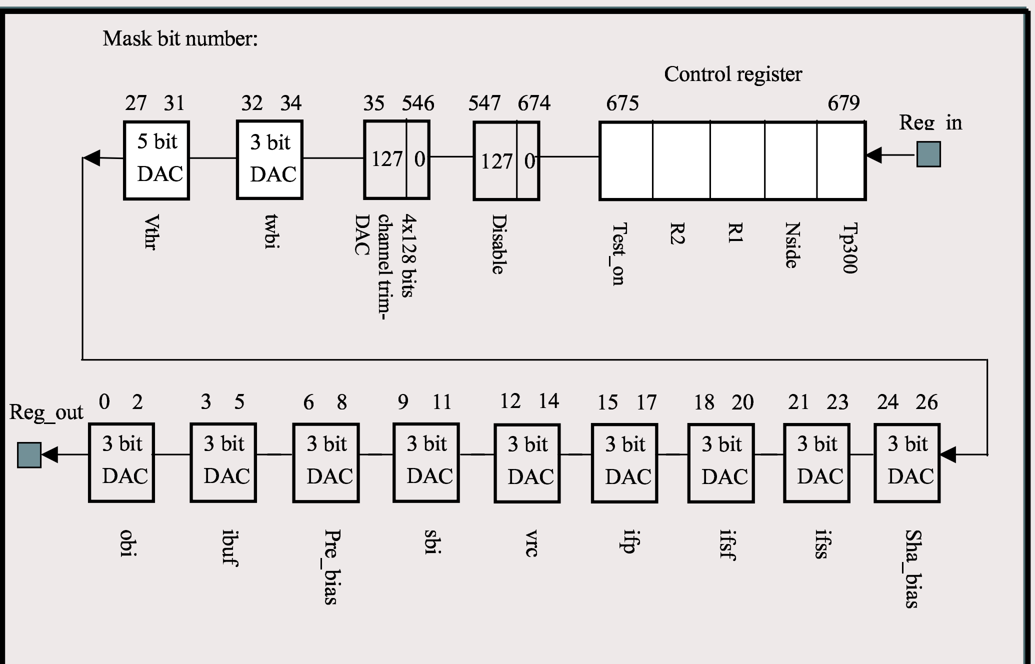
November 21, 2002
SVD meeting

1. Introduction - reminder
2. Target regions
3. Measurements
4. Summary and plans

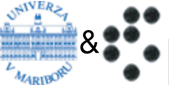
VA1TA schematics





SEU vulnerable parts:

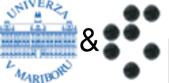
- ✦ shift register for analog multiplexer (128 bit)
- ✦ shift register for chip control (680 bit)



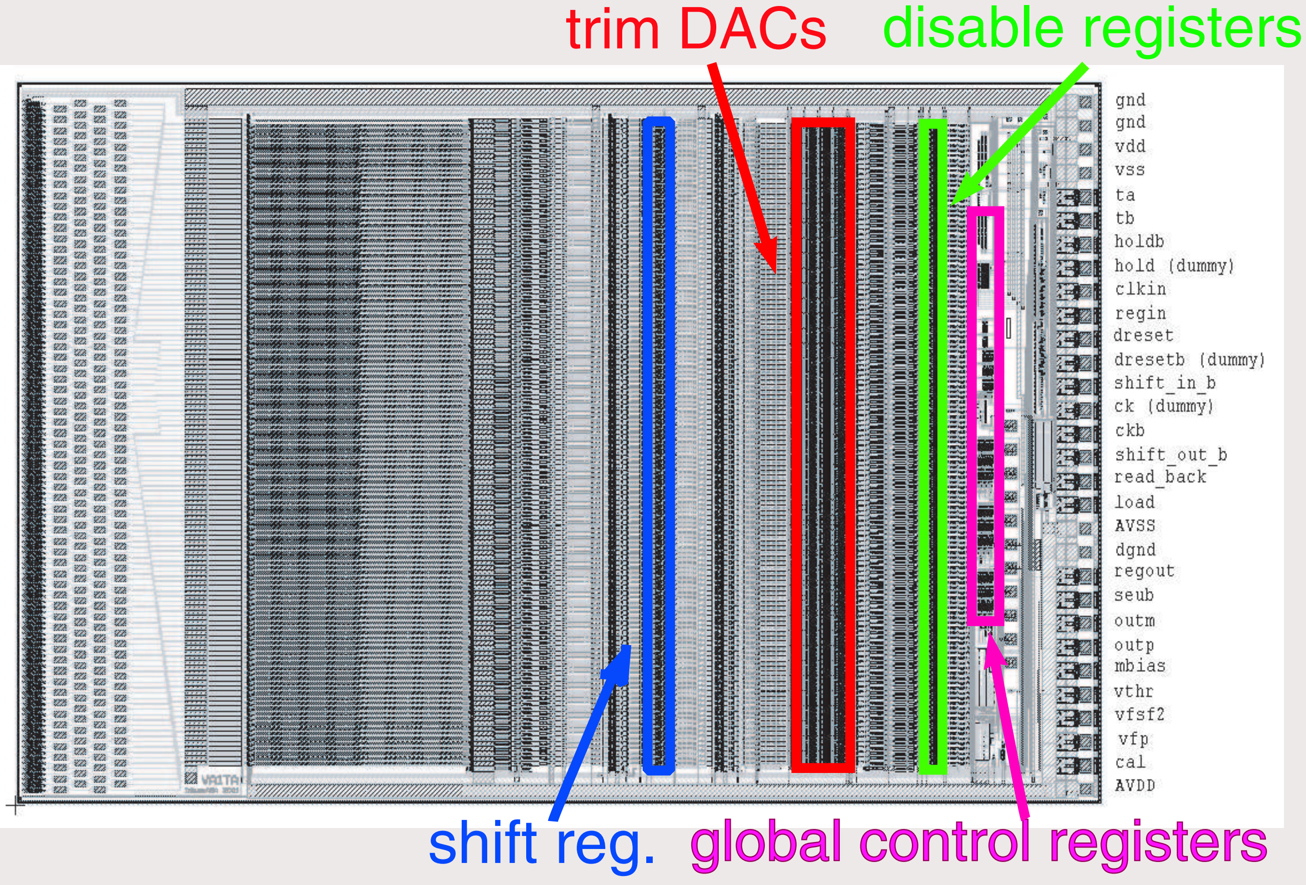
VA1TA SEU detection and correction

Schematics of SEU correction circuit.

- ✦ shift register
- ✦ three parallel latches
- ✦ majority logic for valid bit
- ✦ SEU detection and correction



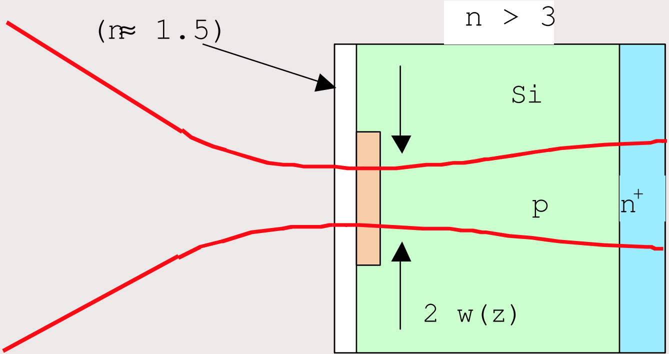
VA1TA SEU sensitive areas



Laser beam characteristics

Requirements for the laser:

- short pulses (less than $\approx 100ps$)
- high energy deposited in active the volume per pulse ($\approx 1pJ$)
- small beam size



Gaussian beam focusing:

- beam size spreading

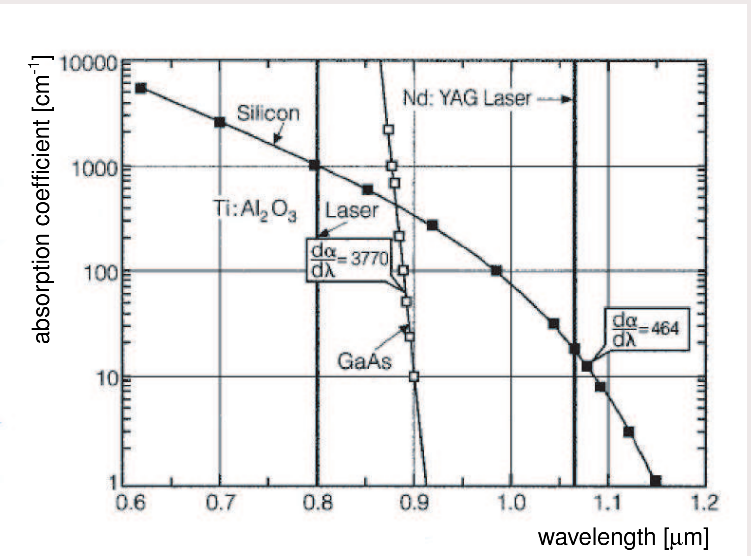
$$w(z) = w_0\sqrt{1+\left(\frac{\lambda z}{\pi w_0^2 n}\right)^2}$$

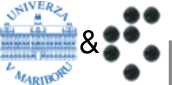
- focus spot size ($w_0 = 2\sigma$)

$$w_0 = \frac{2\lambda f}{\pi D}$$

- depth of focus - Rayleigh range $w(z_R) = \sqrt{2}w_0$

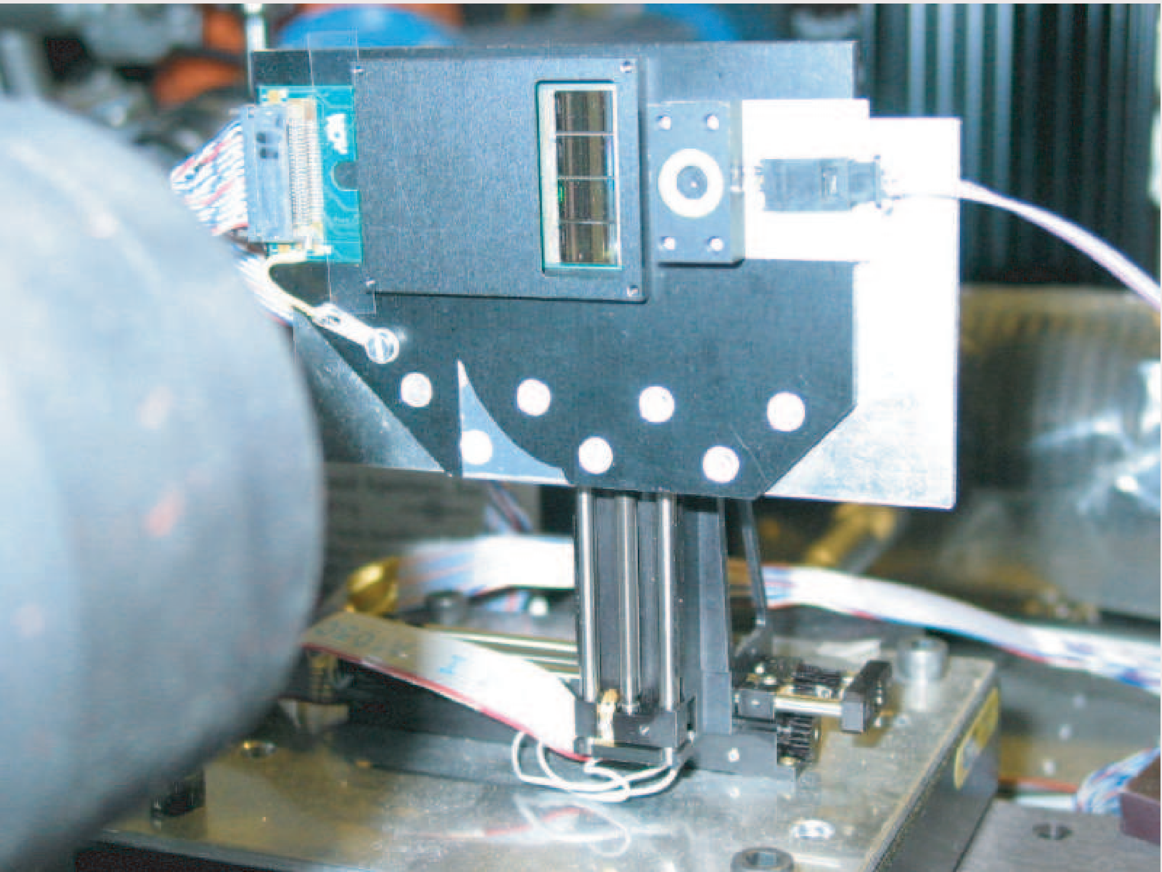
$$z_R = \frac{\pi n w_0^2}{\lambda}$$





Hybrid mounting - 2+1 D

- 2D steering table (x,y)
- 1D manual linear stage
- hybrid
- photo-diode with $100\mu m$ diameter aperture



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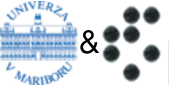
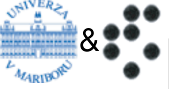


Readout

Monitored parameters:

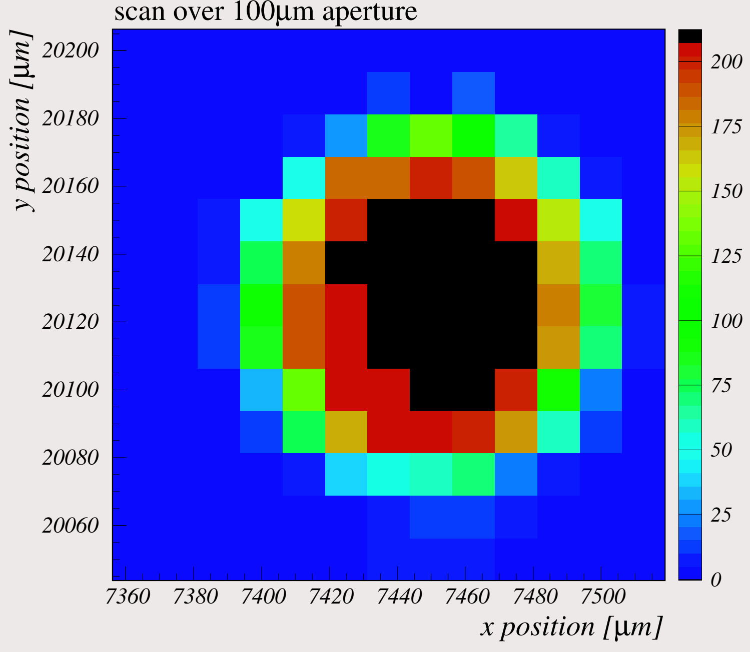
- all bias and supply currents and voltages
- shift register for analog multiplexer
- 8 bit SEU signal counter (255 = overflow)
- shift register for chip control
- state of the valid bits
- photo-diode current

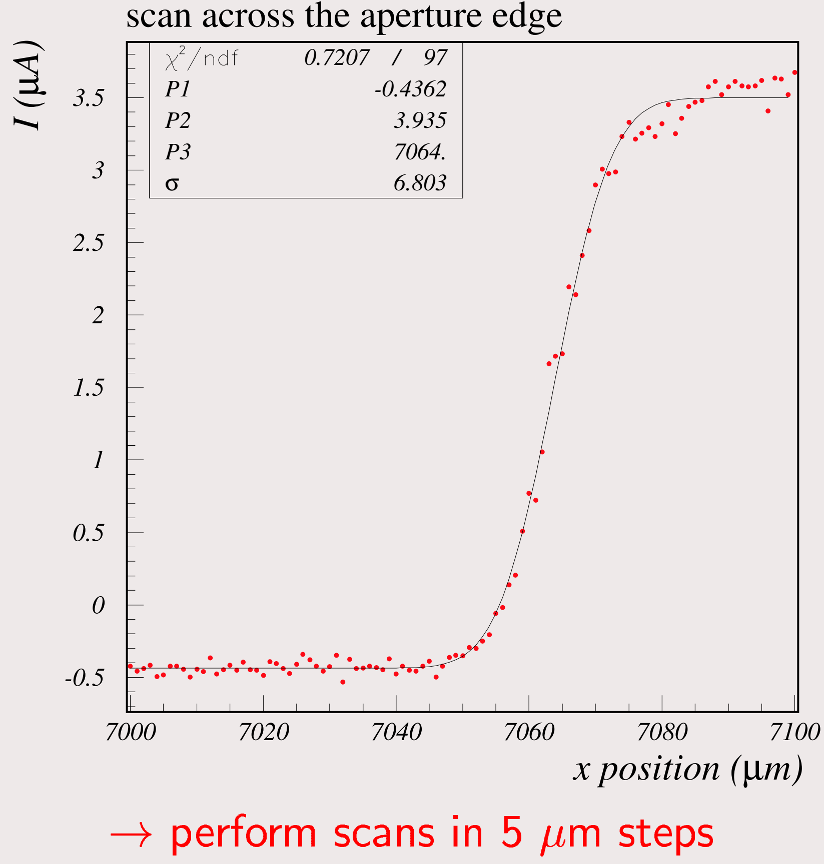


Focus and spot size

Determination of the focus position and spot size by scanning over the photo-diode with $100\mu m$ diameter aperture.

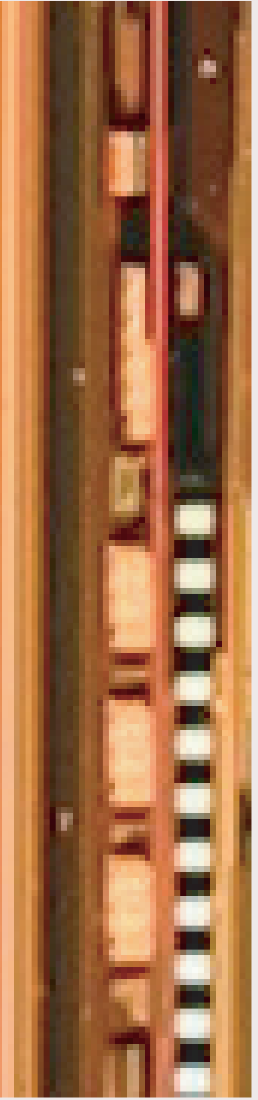
- ✦ $\sigma \approx 7\mu m$ $\longrightarrow$





$\rightarrow$ perform scans in 5 μm steps

Global registers



SEU counter

y position [µm]: 22000, 22500, 23000, 23500, 24000, 24500, 25000

x position [µm]: 29715, 29925

Colour scale: 0, 50, 100, 150, 200, 250

REGOUT errors

y position [µm]: 22000, 22500, 23000, 23500, 24000, 24500, 25000

x position [µm]: 29715, 29925

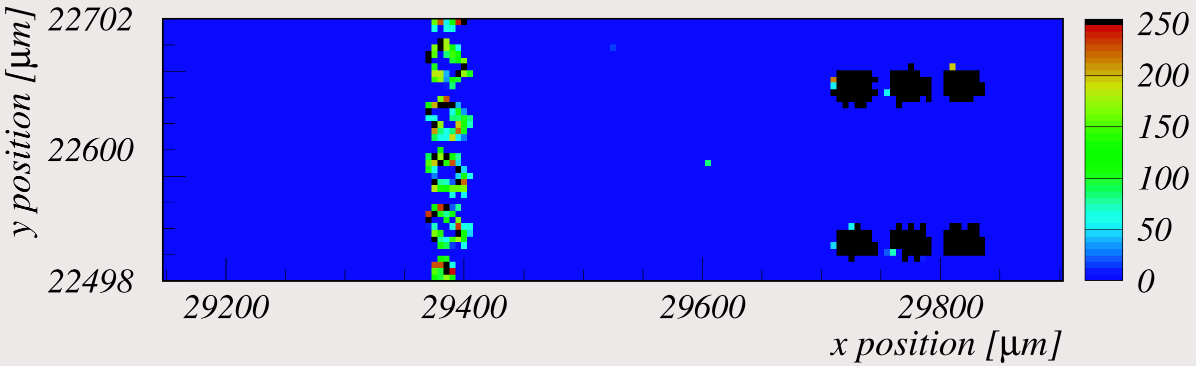
Colour scale: 0, 200, 400, 600, 800, 1000, 1200, 1400, 1600

TA disable and global registers

Test sequence:

- move to position
- reset SEU counter
- wait for $\approx 0.5s$
- read SEU counter
- clock out the chip control register and count the number of flipped bits

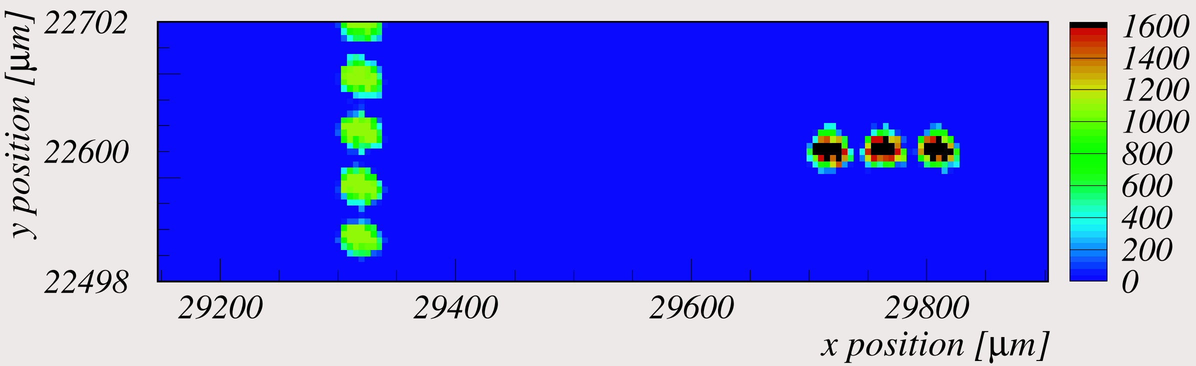
- SEU counter



- all the 0's in the shift register for chip control (REGOUT) that pass the laser point are flipped to 1

$$0 \rightarrow 1$$

- REGOUT errors



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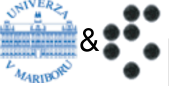


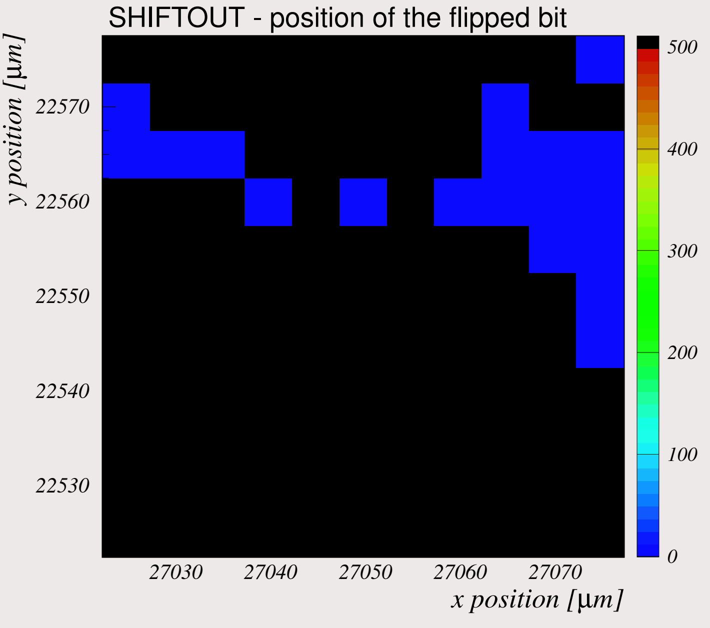
SHIFTOUT errors

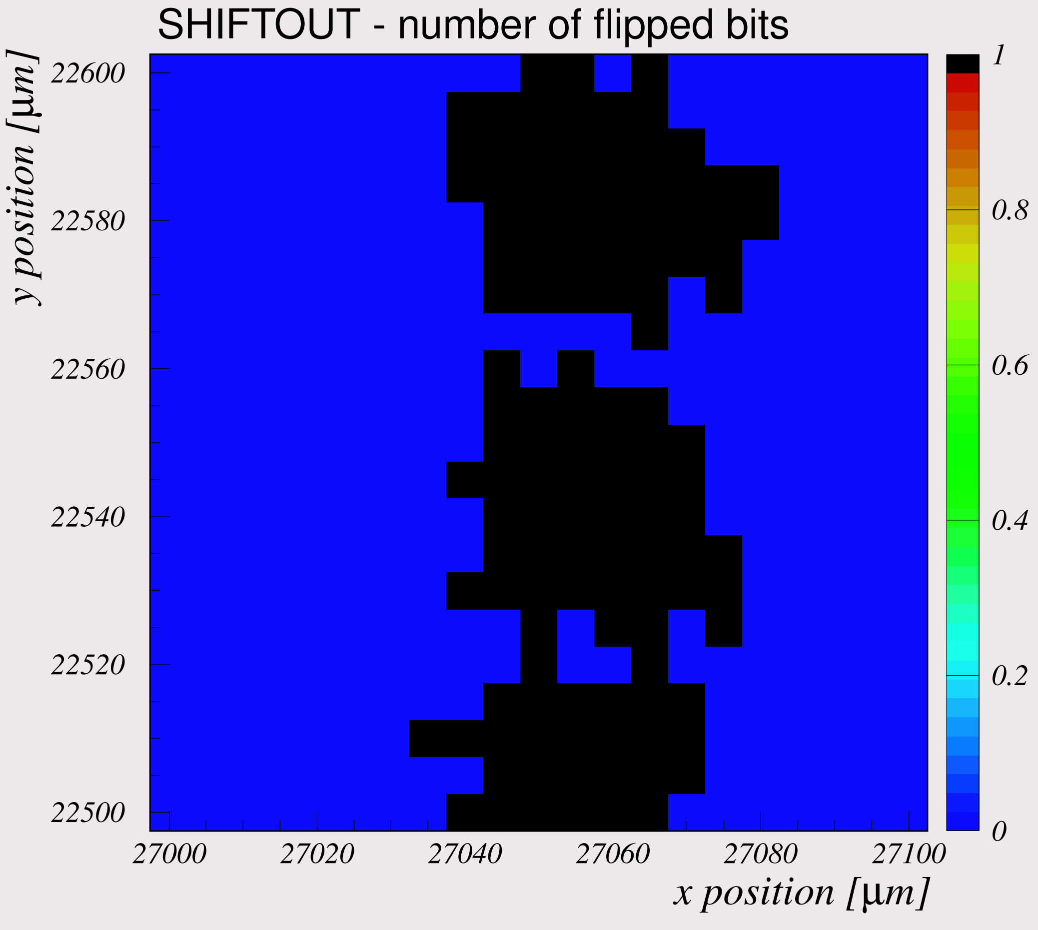
Test sequence:

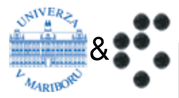
- ✦ move to position
- ✦ reset of shift register (all bits 1)
- ✦ clock one bit (0) thru the register and count the number of flipped bits

- ✦ 0 bit flipped to 1

$0 \rightarrow 1$

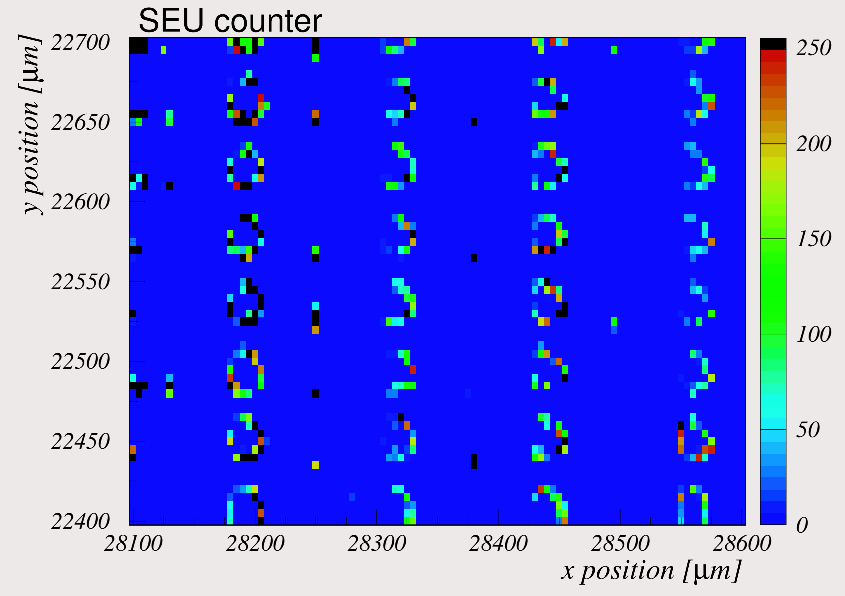


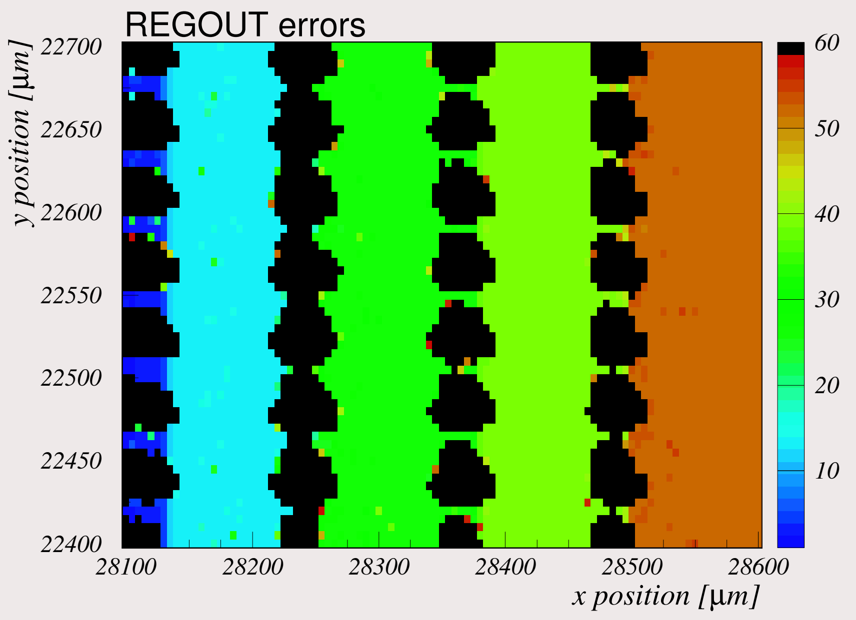


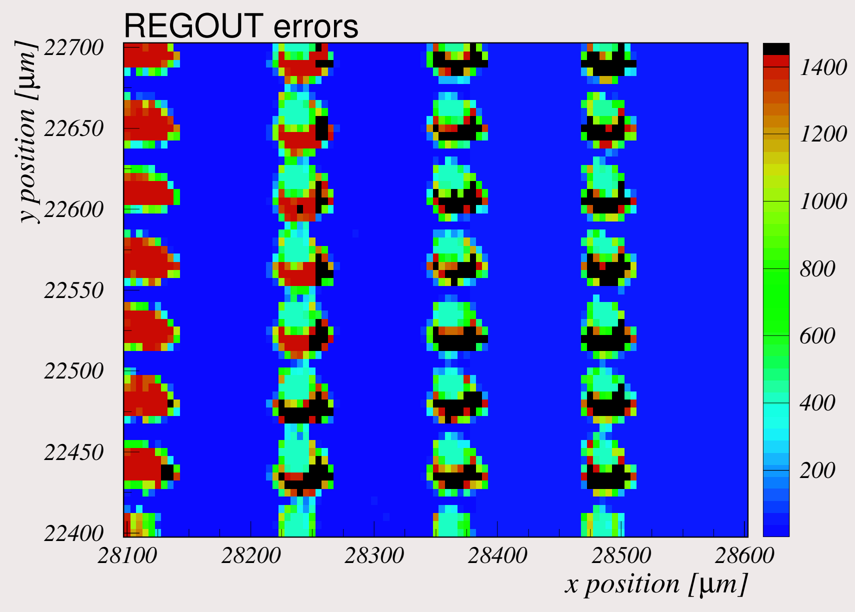


Trim DACs

- scan over the trim DACs area with higher pulse energy
- permanent change in chip control register observed

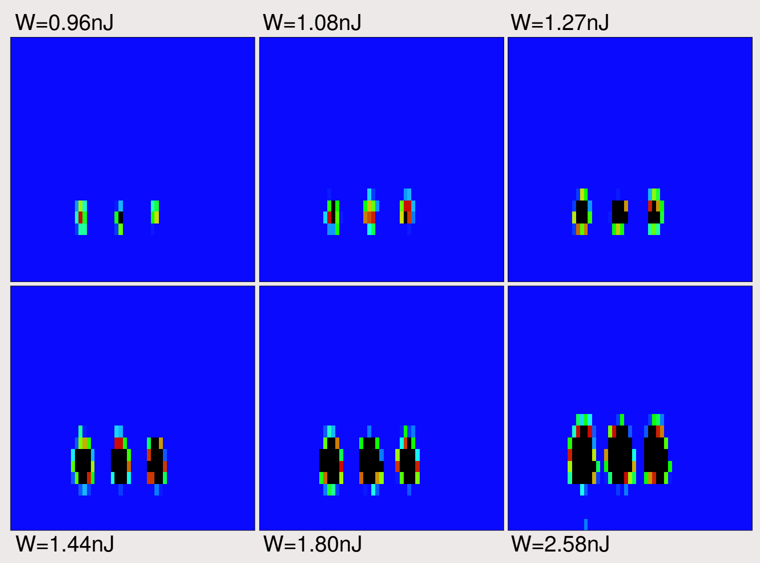


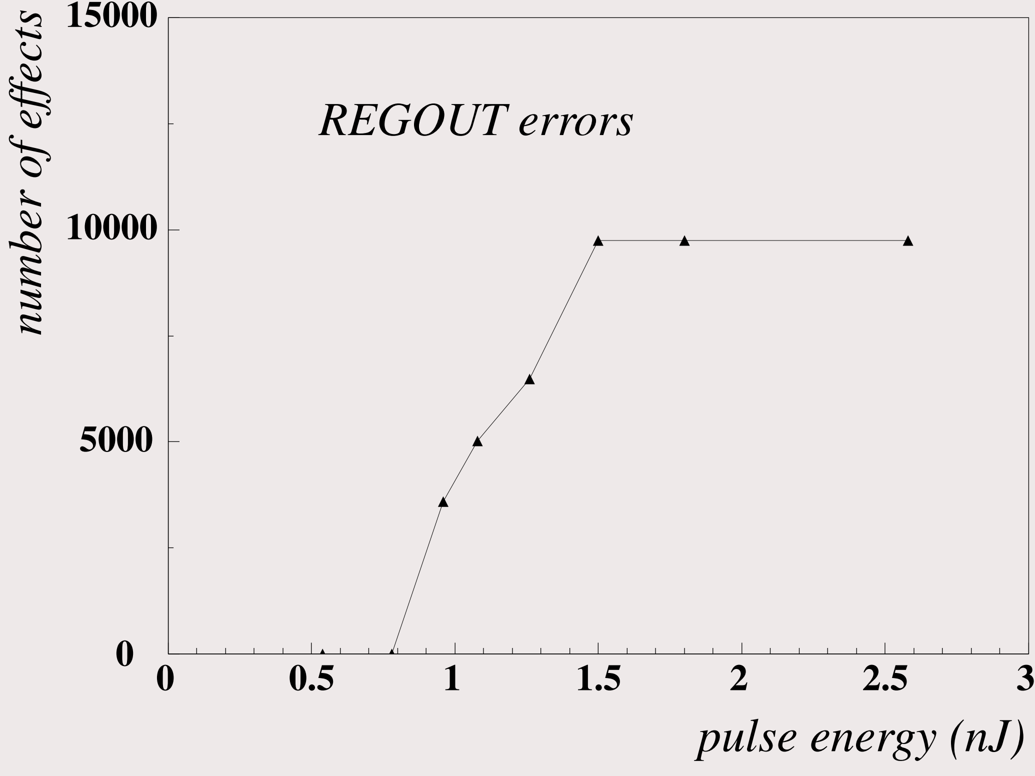




SEU threshold - REGOUT errors

- number of the REGOUT errors as a function of the pulse energy





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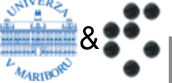
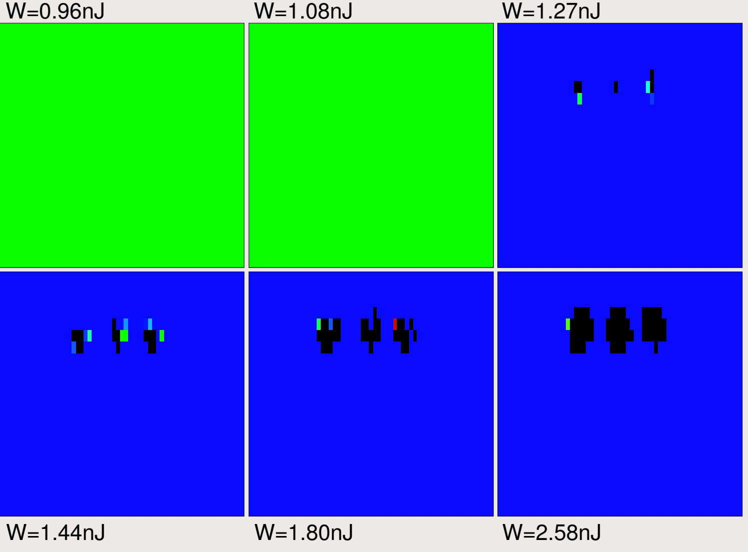
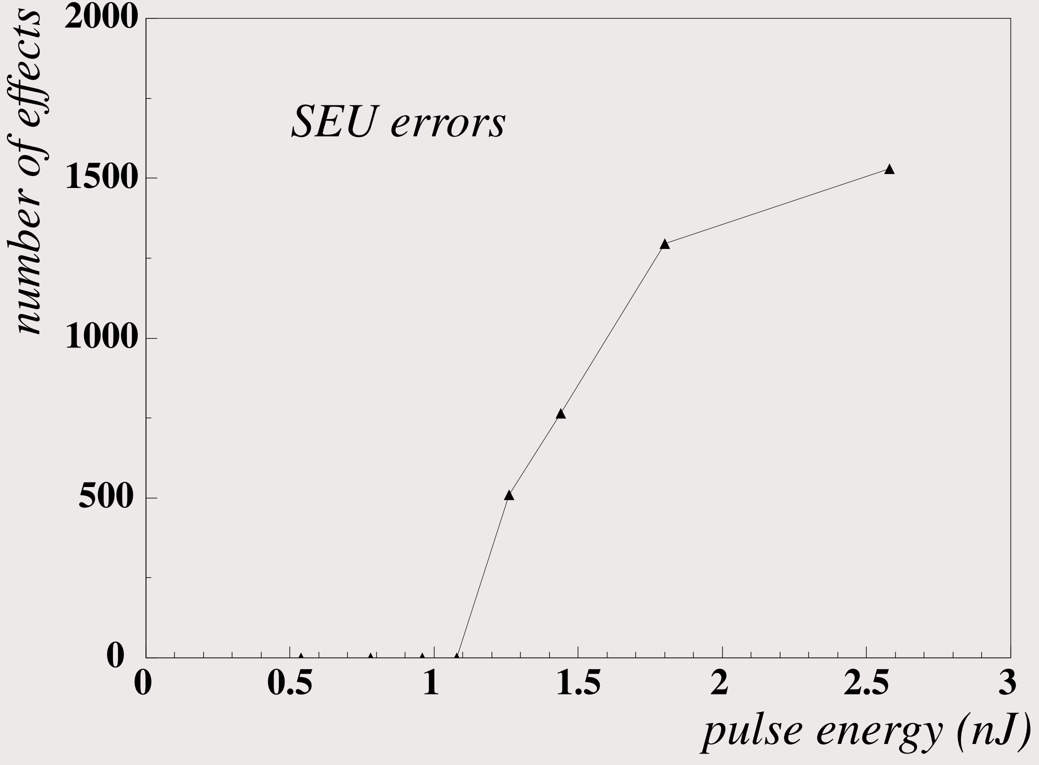
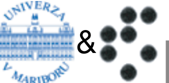


SEU threshold - SEU counter

- number of the SEU pulses as a function of the pulse energy







Summary and plans

- Setup for the SEU testing with laser has been constructed and is now being routinely used
- potential SEU sensitive spots were identified and compared with the chip layout

Next steps:

- get a detailed layout (discussed with IDEAS - Bjorn and Sindre)
- go to a smaller spot size (using an additional beam expander)
- clarify open questions (permanent chip control register change)