VA1TA TESTING FOR SINGLE EVENT EFFECTS - STATUS

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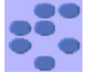
May 15, 2002
SVD2 Upgrade Meeting, Princeton

- VADAQ modifications
- High power laser scanning
- SEU monitoring

VADAQ calming down - update



- The ringing in the trigger section was filtered out
- The problem we saw seems to be entirely on the VADAQ side - did not occour on the VADAQ Samo used at KEK

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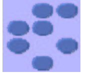
SEU monitoring



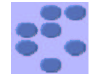
Status as of my last report in March:

- No information on the *seub* value in VADAQ software.
- Therefore: we have to dig out this information from the VADAQ.

In the meantime it became clear that

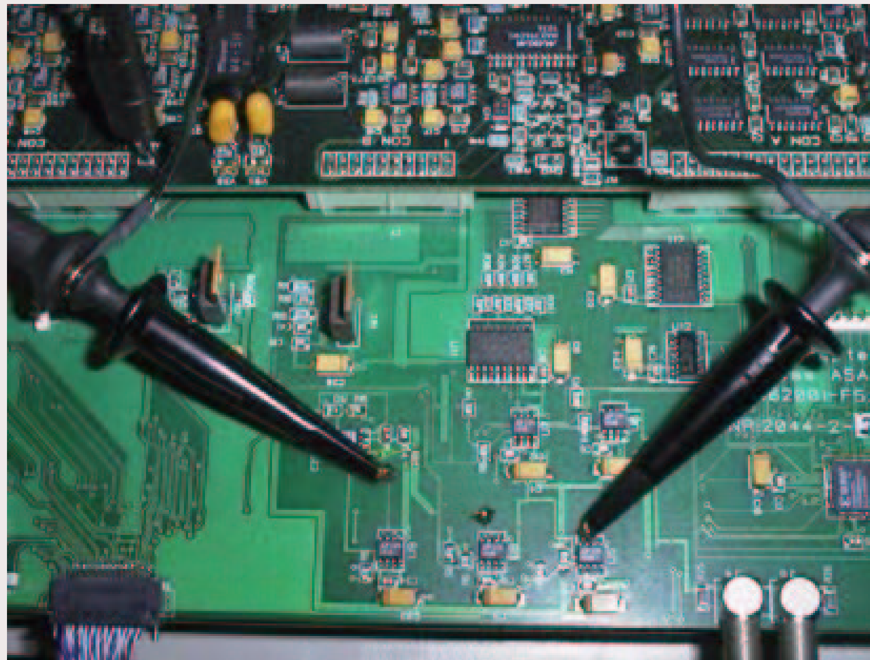
- No information on the *seub* value is forwarded into VADAQ hardware in the current version (stops in the input Xilinx chip)
- *seub* output signals are asynchronous with the read-out clock, and thus cannot be extracted in the same way the read-out is performed.
- We have to monitor shift out as well to check whether the read-out chain was affected

Input Xilinx programming 1



→ Reprogramming of the Xilinx chip is necessary!

seub input to VADAQ



Xilinx chip programming connector

Xilinx input/output chip

Reprograming is done by using the Xilinx instructions (on the web), through a dedicated parallel port → VADAQ connector cable ('Xilinx cable nr. 3' or nr. 4).

Since we had little time, we ordered cable nr. 4, but built nr. 3 (which was then essentially used).

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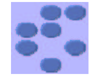
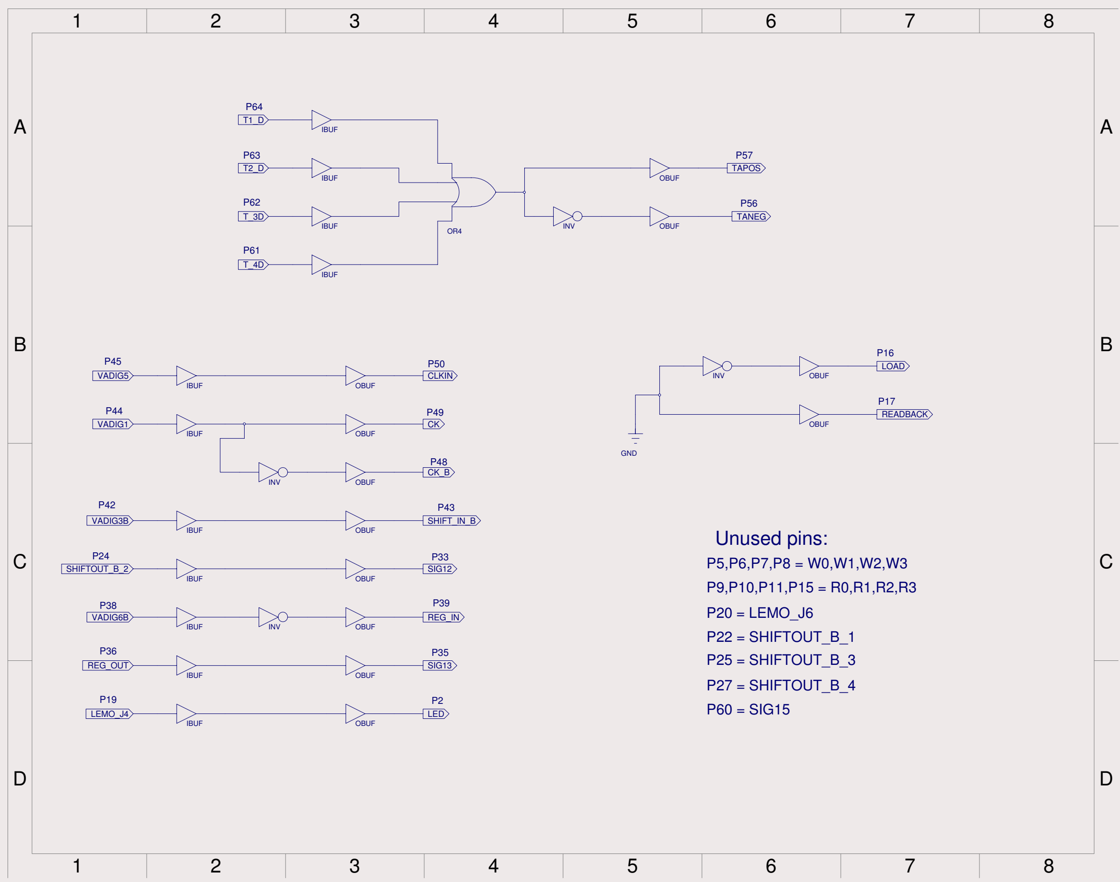
Original Xilinx program in our VADAQ version



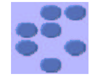
- shift out of the second chip is returned
- load register all the time on, read-back all the time off



$\longrightarrow$ independently of SEU occurence

- no SEU output signal enabled
- no check of the register content possible

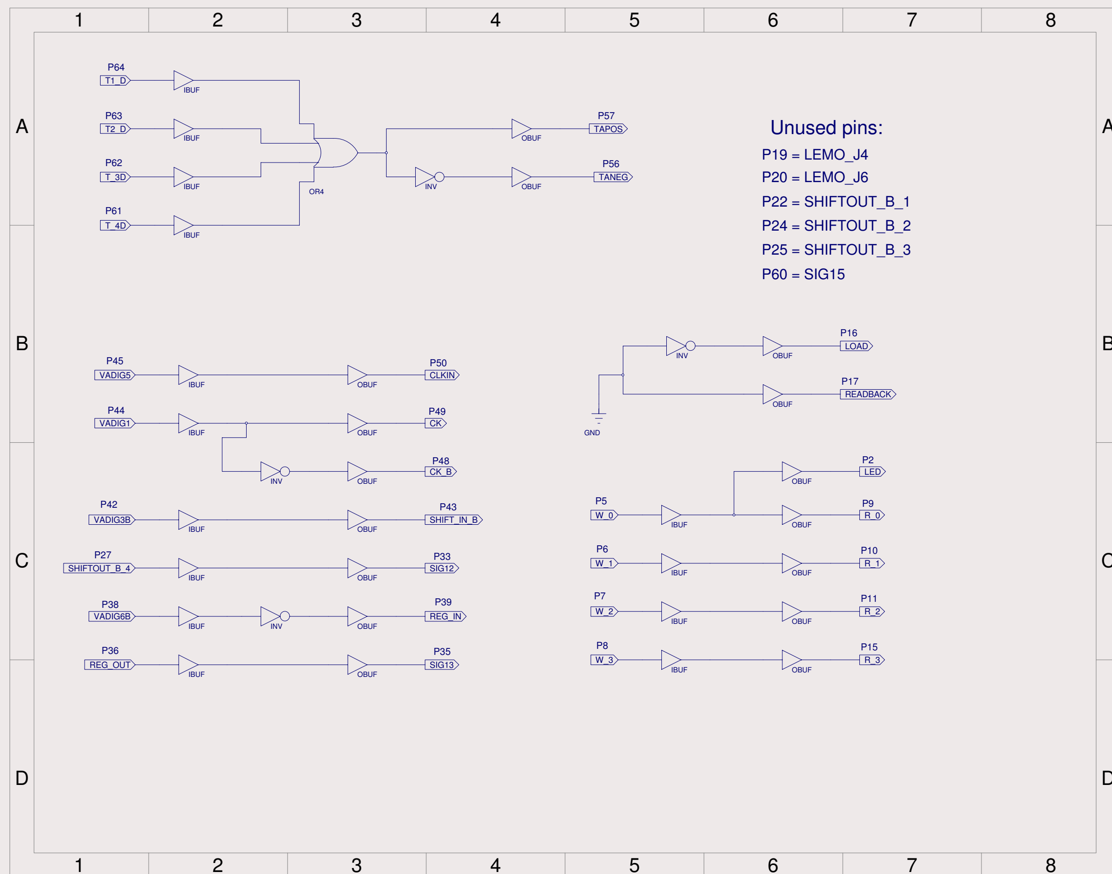
Input Xilinx programming 2



First try to check whether we understand how to do it, and make a very simple change:

- shift out of the fourth chip is returned
- connect the user defined read (R_i, i=0-3) and write (W_i, i=0-3) lines
- LED lights according to the first bit (R_0)

→ works!



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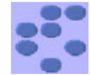
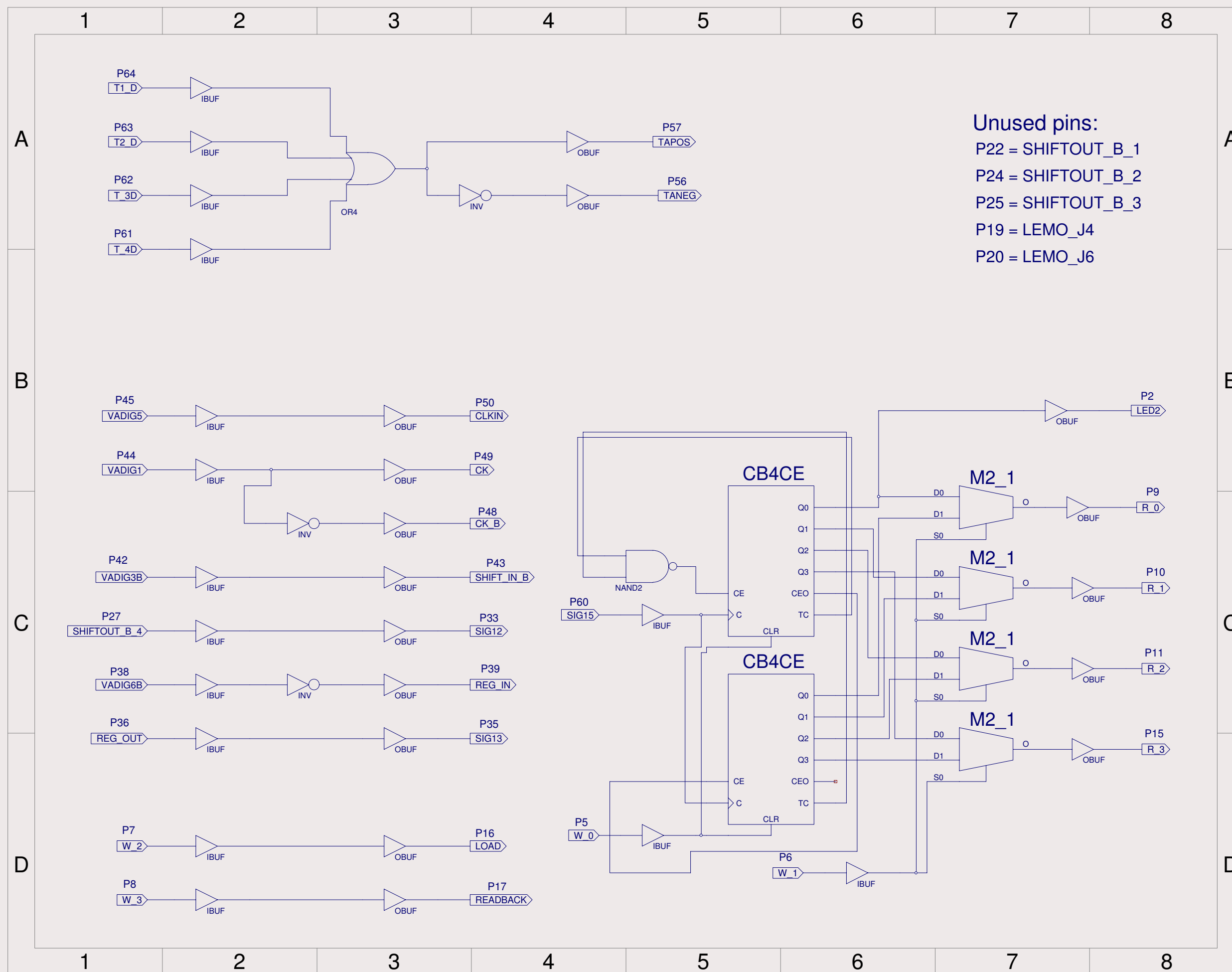
Xilinx programming 3: SEU monitoring scheme



- shift out of the fourth chip is returned
- SEU counting is done in the Xilinx chip (counts until 255)
- LED lights up according to the first bit value, stays red at overflow



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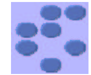
Input Xilinx programming 4



One more possible use: Implement the parallel read-out of the four chips by reprogramming the Xilinx

Unused pins:

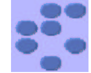
P7,P8 = W2,W3

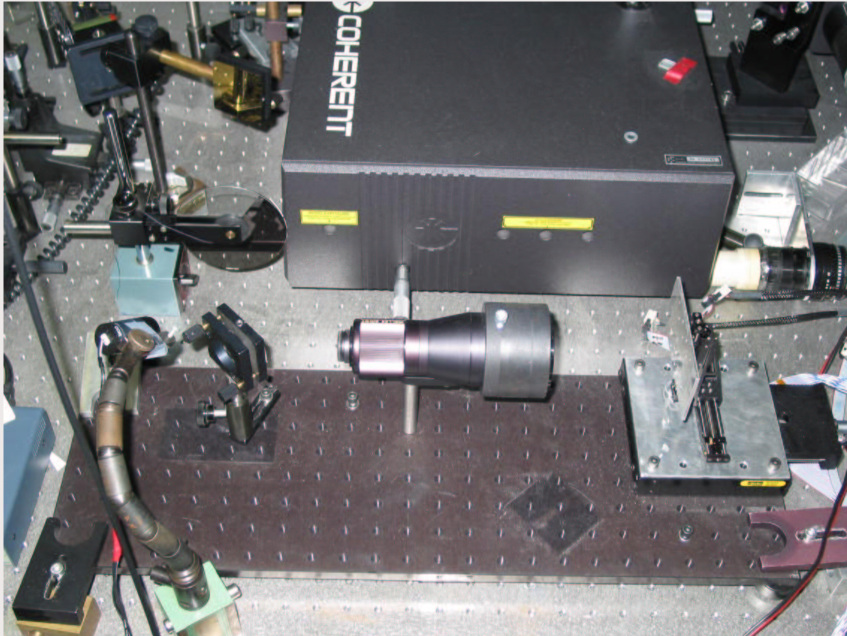
P9,P10,P11,P15 = R0,R1,R2,R3

P20 = LEMO_J6

P60 = SIG15

Back to the high power laser set-up





Set up in the optics lab:

- pulse frequency: 250 kHz
- pulse width < 1 ps
- energy per pulse after a 10^3 attenuator: 120 pJ
- further attenuation: 1-1000

Contrary to expectations (we anticipated problems because we are parasitic users, less infrastructure), we managed to arrive at a very good arrangement - we are even allowed to start the laser on our own.

New scanning/DAQ software to include SEU counting, shift-out checking, allow for both x,y and y,x scans.

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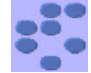
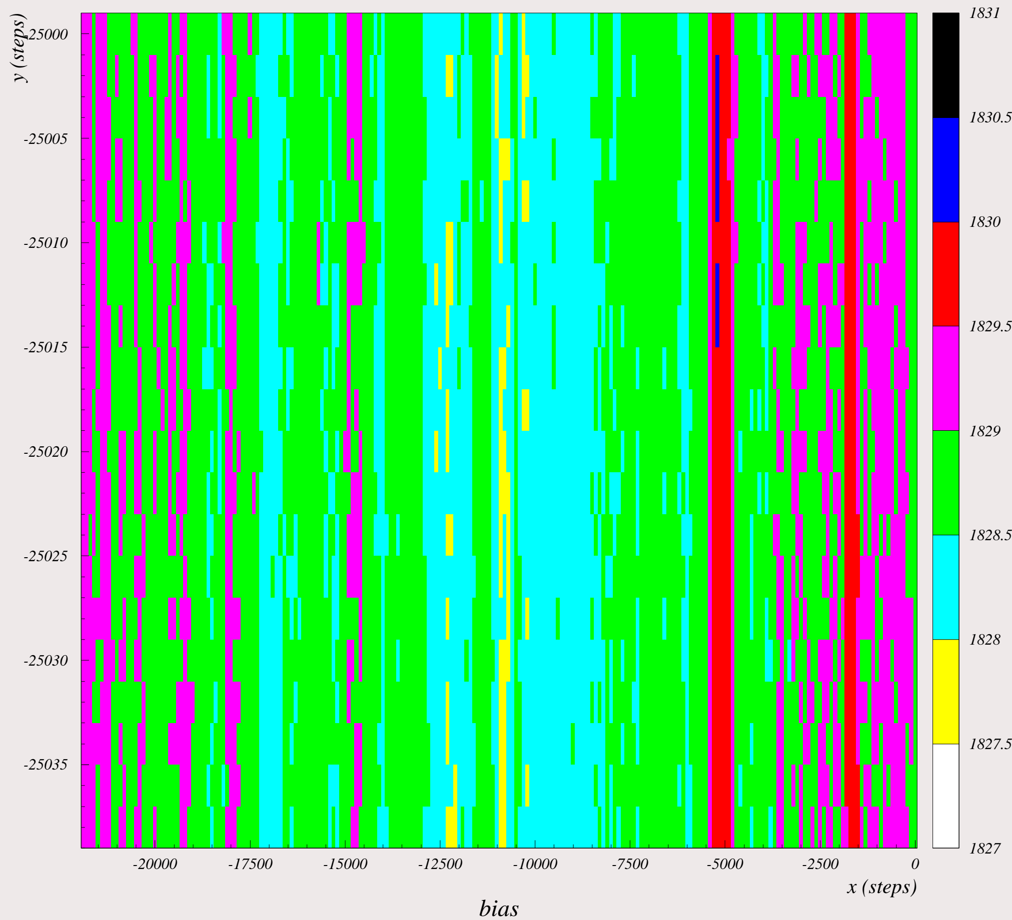
VA1TA scan with high power laser



Mbias vs. x,y over the full chip length (9 mm), 1/2 read-out channel (20 μm) in y



No shift-out failures!

SEU counting was not implemented yet in this scan

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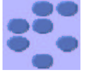
Focus, positioning



To find the focus, sensitive spots (areas where one of the currents - say mbias - increases) have to be found, and scanned over in small (1 μm) steps. Plane of the chip is in the focus when edges are sharp.

Positioning: relative to hot spot edges.

How do hot spot reactions depend on exposure history, intensity?

How constant is the input beam position?

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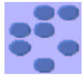
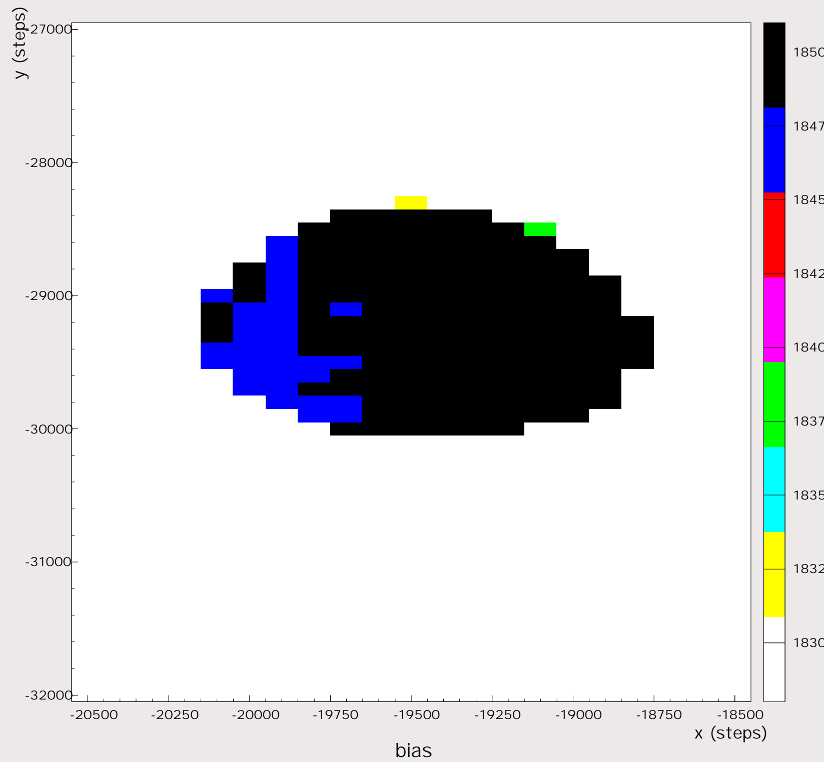
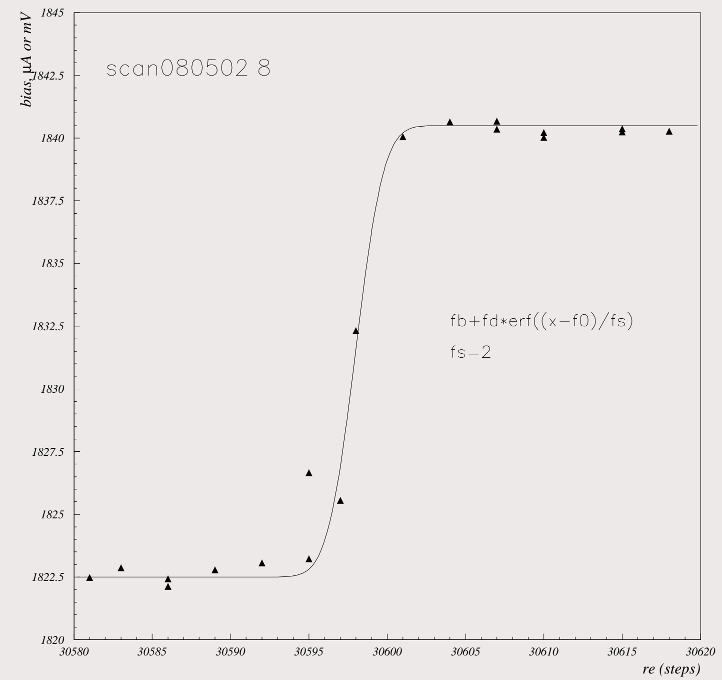
Focus



Hot spot, found with coarse granularity scans



Scanning over the edge of a feature



2 steps = 1 μm

Control register

The Va1Ta chip contains a 680 bits long shift register which can be loaded serially using *RegIn* (serial data) and *ClkIn* (clock). A more thorough description of the contents of the register is found below and in figure 9.

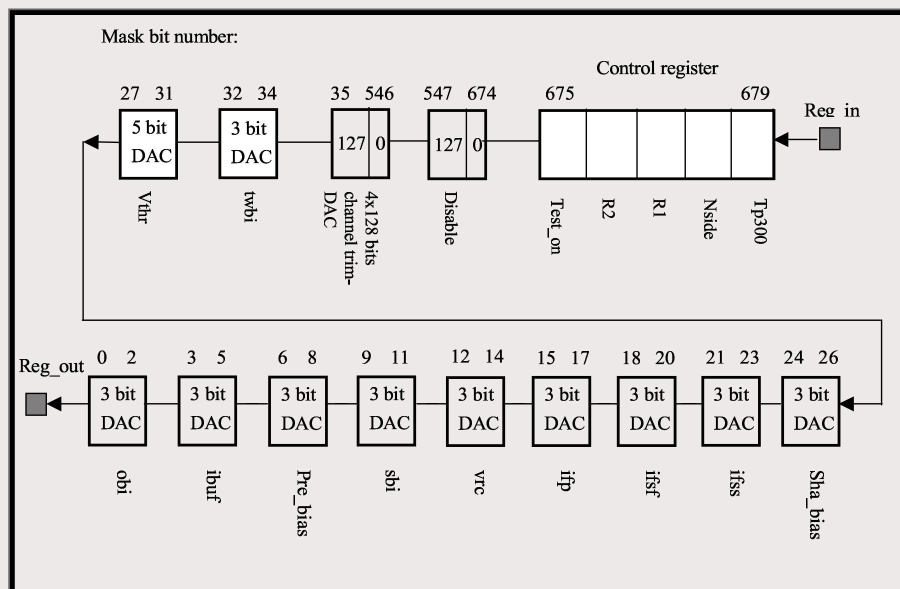


Figure 9: The sequence of the serial shift register mask. The sequence numbers are shown at the top of the boxes. Bit 0 is the first bit to be loaded. The channel numbers are indicated inside the boxes for the channel disable register and the channel threshold DAC register.

The serial shift register is shown in figure 9. The bits in the control register have the following function. A "1" in *Tp300* sets the peaking time of the fast shaper to 300ns. "0" sets the peaking time to be 75ns. A "1" in *nside* will prepare the channel for negative input signals. This control signal affects both bias generation and channel logic. The bits *R1* and *R2* controls the feedback resistor in the preamplifier, and are described in table 1. In test mode, the *test_on* –bit must be set (in addition to a bit in the *test enable* –register). The channel *disable* –register disables any channel with a high bit.

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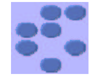
SEU scheme



Serial shift register structure

The serial shift register used for slow control is implemented with flip-flops specially designed to be SEU tolerant. A schetch showing the principle of these cells is shown in figure 8. Bits are shifted into the cell through the *D* pin into the D-flip-flop by applying pulses at the external clock pad. The output of the DFF is shifted out through the *Q* output pin. When all bits have been shifted to the correct place in the serial shift register, a pulse should be applied to the *load* pin. This will open the latches, and store the value of the DFF in the three parallel latches. The stored values in the latches are seen by two different blocks of sequential logic. The *Majority selection module* outputs the logic value that the majority of the latches store. This logic value is the value that is actually used by the chip logic, and is output through the *valid bit* pin.

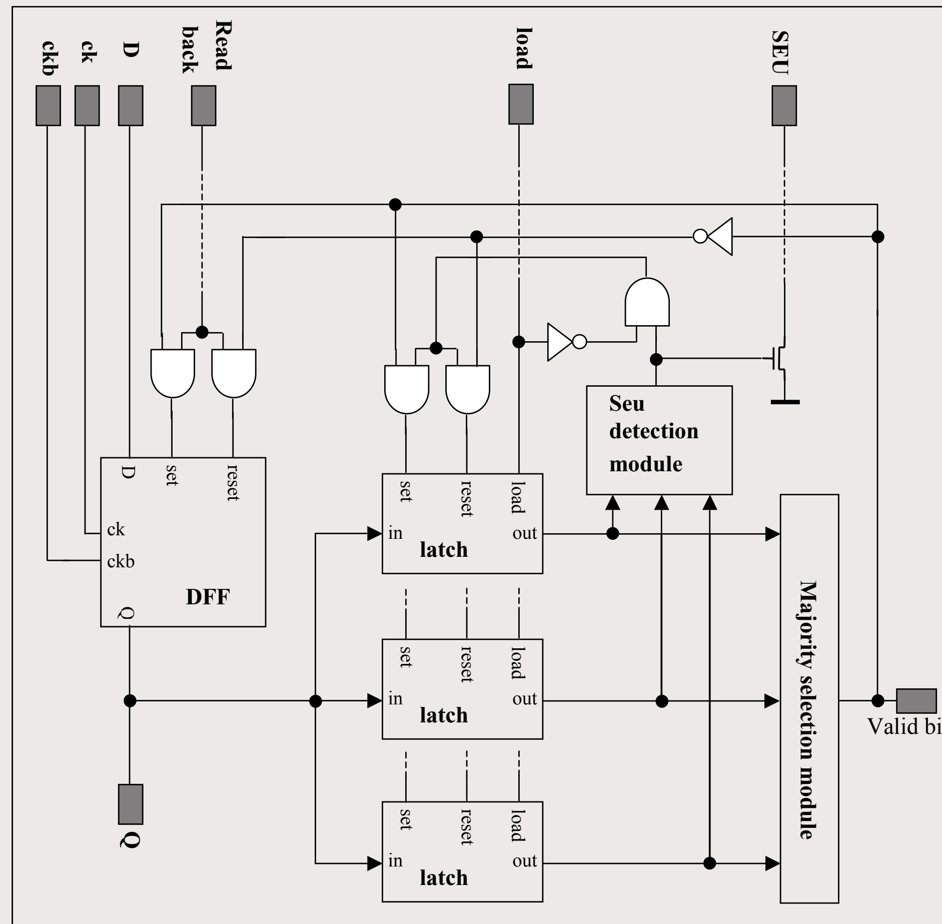


Fig. 8: Overview of the architecture of a SEU-flip-flop.

Ideas ASA, Veritasveien 9, Box 315, N-1323 Høvik, Norway

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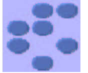
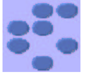
Summary



- High power laser operation has become routine
- Read-out chain is stable
- VADAQ was adapted to the SEU testing requirements
- Positioning is under study
- More scans targeting at possible sensitive areas are under way
- The SEU monitoring scheme is being prepared for the final read-out

More slides, more plots etc



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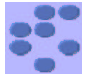
Hybrid case



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