UNIVERZA V LJUBLJANI

VA1TA testing for single event effects - status

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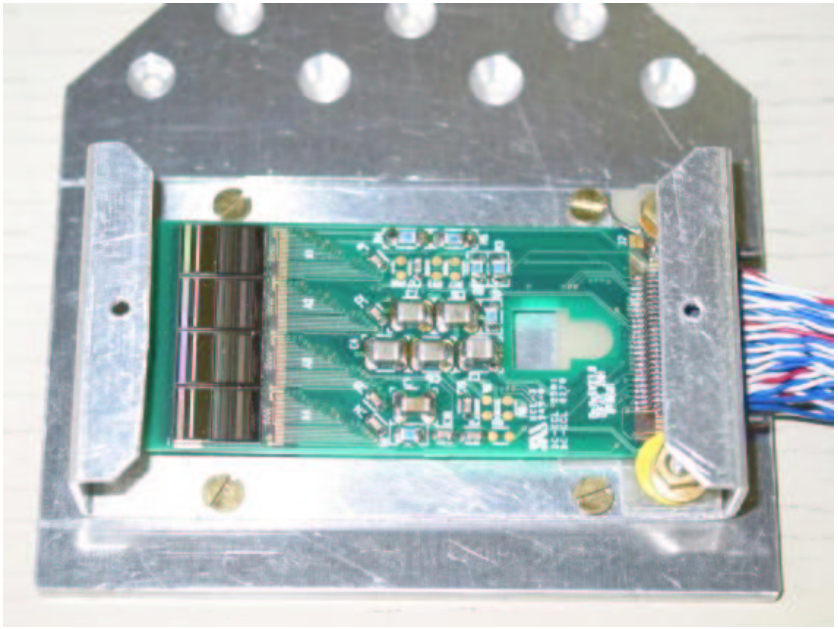
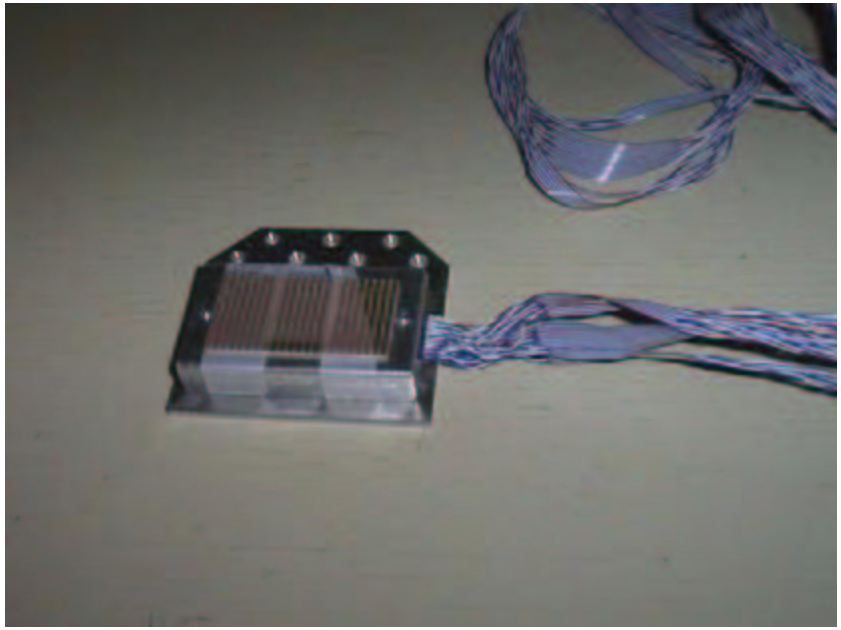
SVD parallel meeting, Mar. 7, 2002

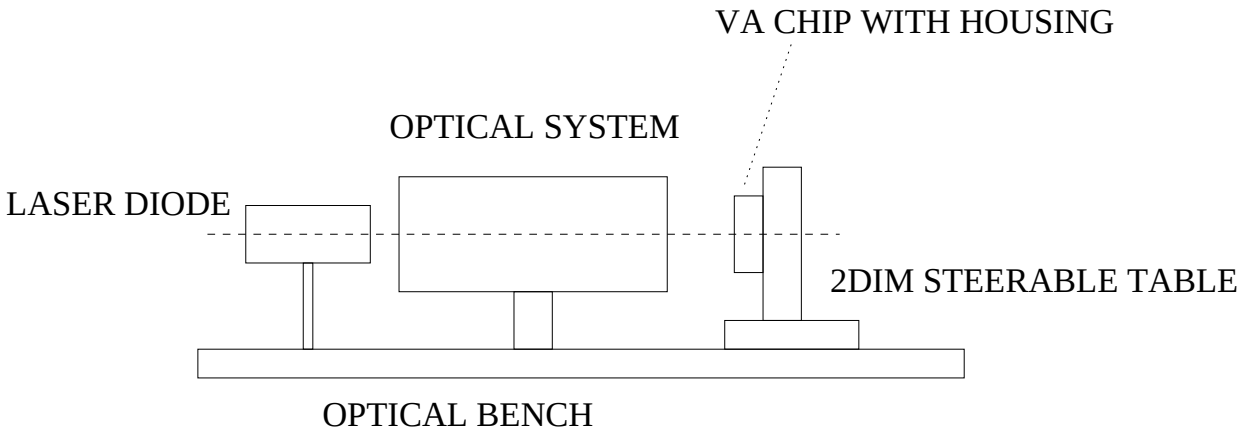
- VA1TA scans with bias monitoring - continued
- medium power → high power laser
- *seub* output monitoring
- some more experience with VA1TA operation
- what is *seub* good for
- plans

Hybrid case and cabling





Medium power laser measurements

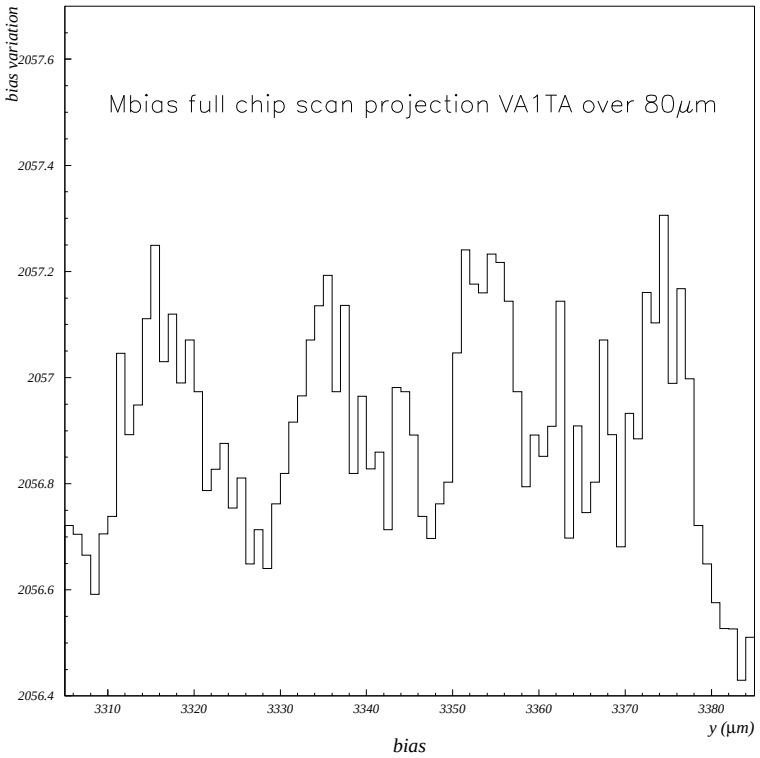


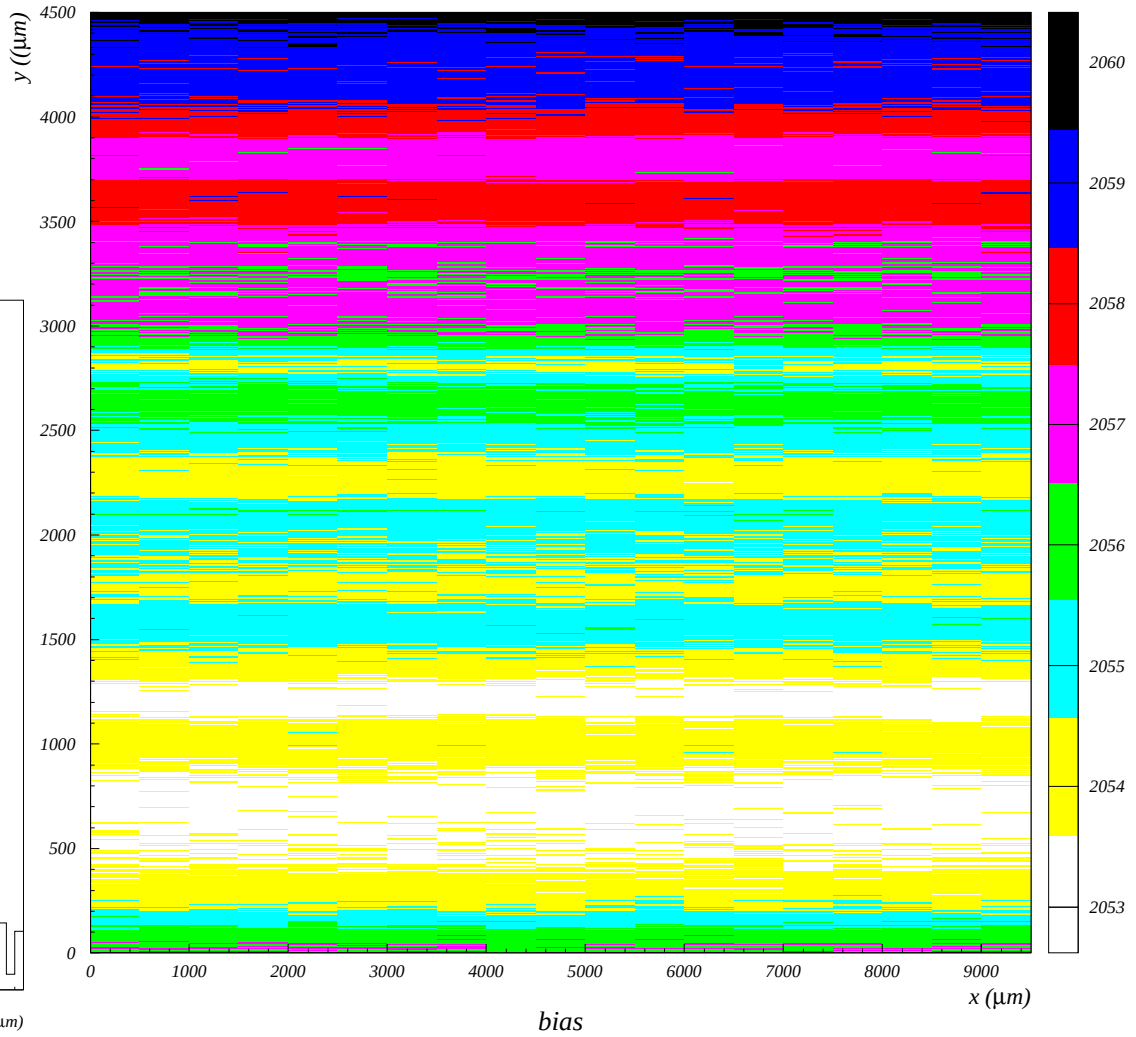
- VA1 scanned in October/November, VA1TA was first scanned just before the November meeting.
- More scans were performed in December, including a full scan over an entire chip over Christmas holidays (10 days).
- All tests: use medium power laser, record bias values.
- $\rightarrow$ Resolution (sharpness of observed features) similar to the VA1 test, order few microns.
- $\rightarrow$ No single event latch-up observed (as persistent current increase).

Medium power laser measurements 2

Scan over the full chip:
Mbias vs. x,y →

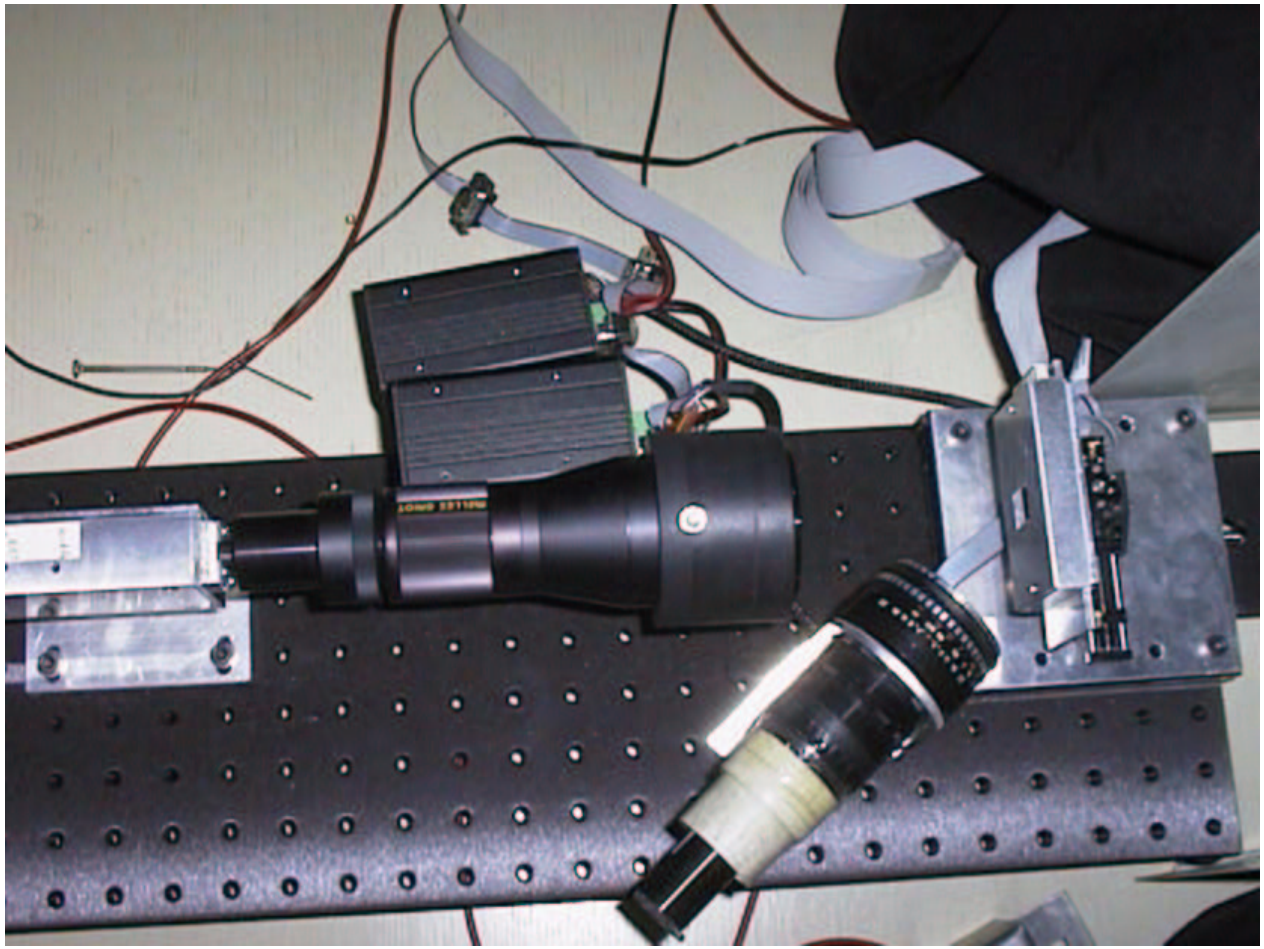
y projection





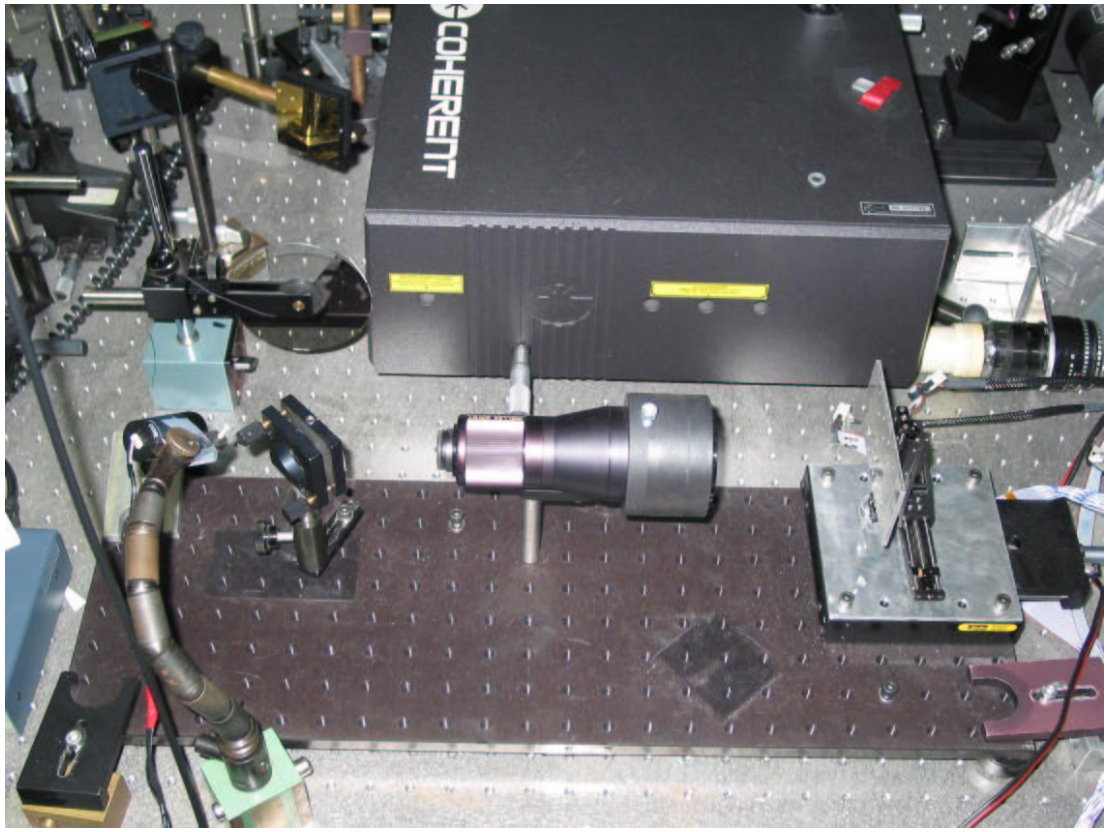
Medium power laser set-up

pulse width 2 ns,
energy per pulse $\approx$ 6 pJ



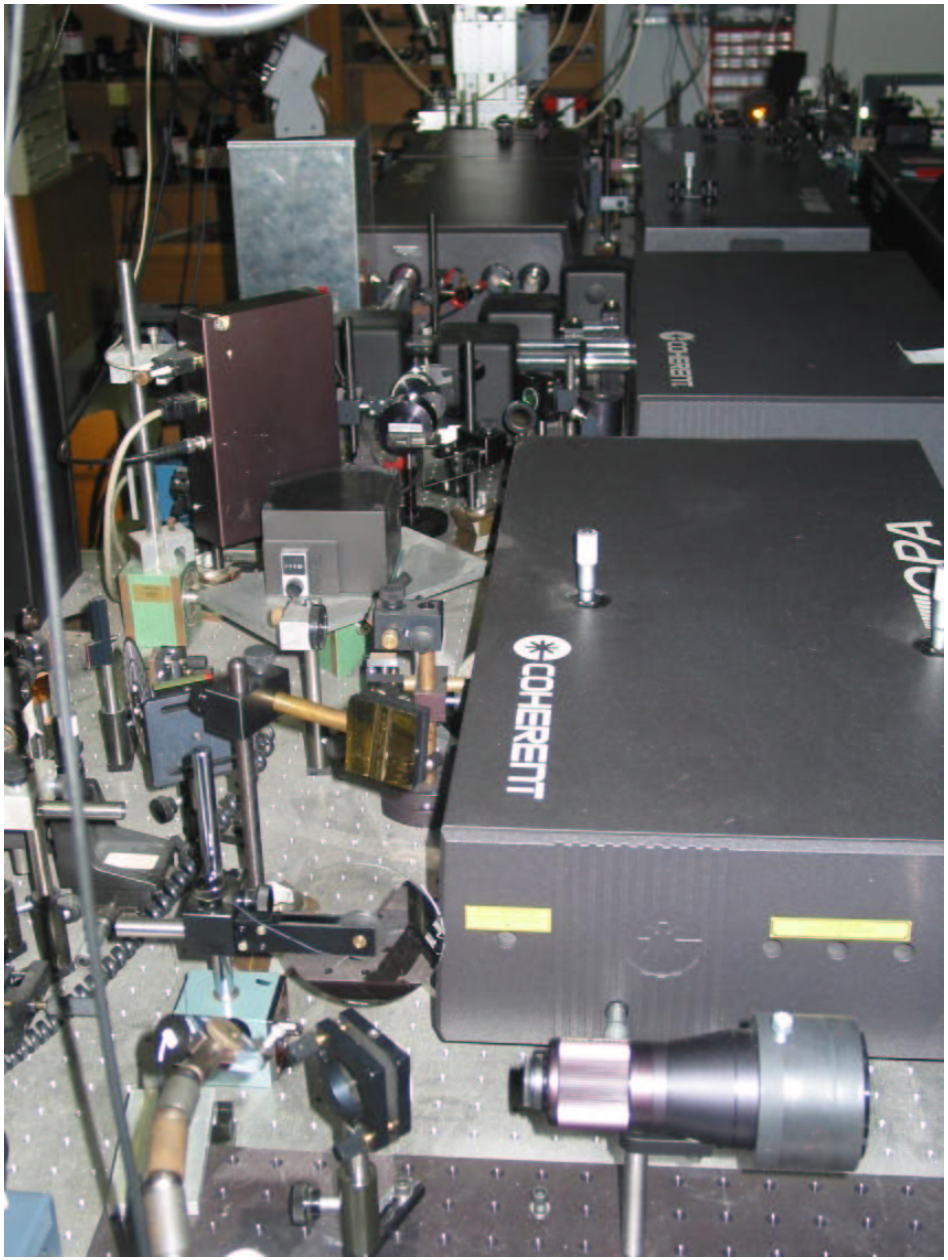
Very useful for tests, but slightly too low in energy per pulse.

High power laser set-up



pulse frequency: 250 kHz,
pulse width < 1 ps,
energy per pulse after
a 10^3 attenuator: 120 pJ,
further attenuation: 1-1000

Enough energy/pulse but in another lab, shared users, less infrastructure.



< – laser exit

< – fixed attenuation 1000

< – variable atten. 1-1000

< – beam expander, focus

High power laser studies - status

- moved to the solid state lab mid January
- optical path aligned
- first try with pulse energies between 1 and 100 pJ

Understanding the TA part in the VADAQ

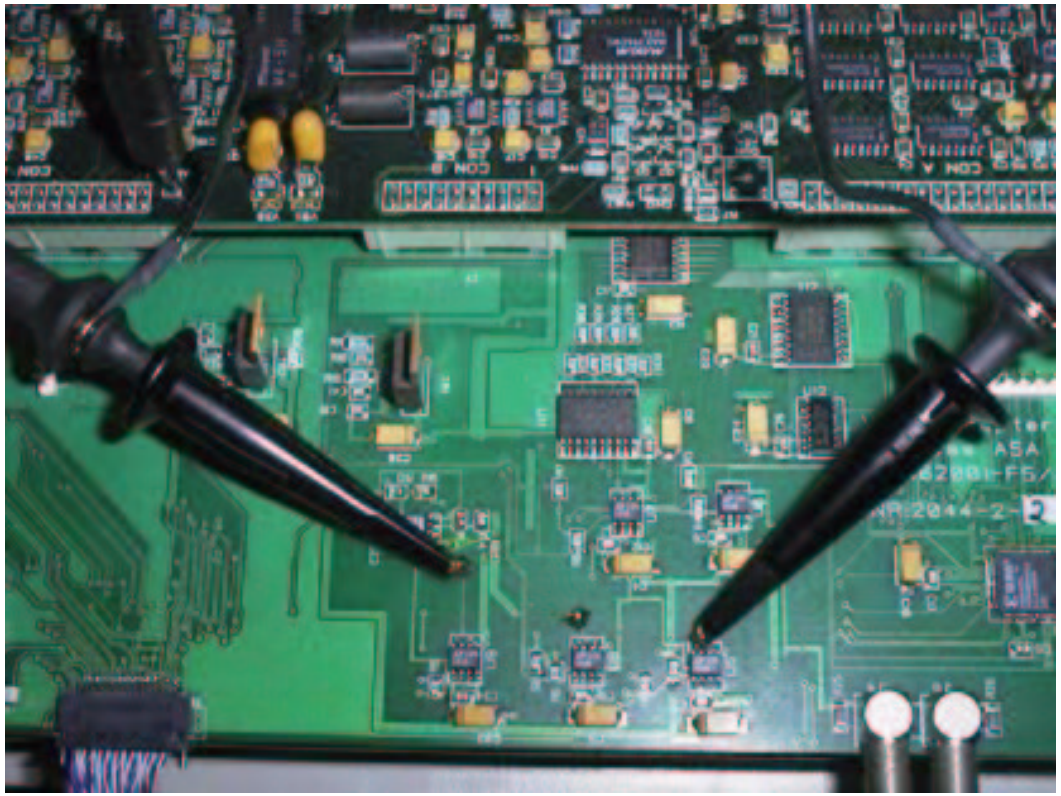
- TA part turned out not to be initialized properly
- $\rightarrow$ move the read-out part back to our lab
- by comparing our VADAQ library with the Tokyo version (same name + version number), we found out that theirs initialized the TA properly

- first experience with the initialized hybrid: ringing without any signal
- try to understand the problem - directly linked to the SEU monitor.

seub output monitoring

No information on the *seub* value in VADAQ software.
Therefore: we have to dig out this information from the VADAQ.
One obvious way to start with: check the output of the corresponding comparator.

seub output



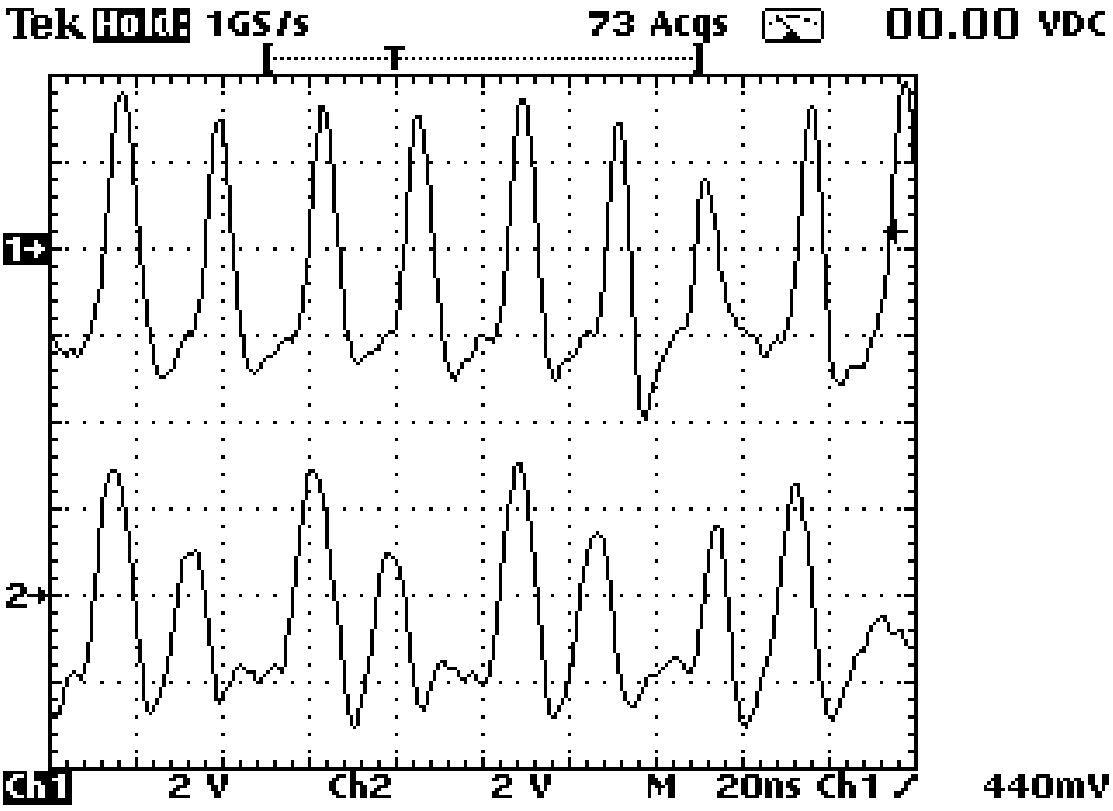
T1 trigger output

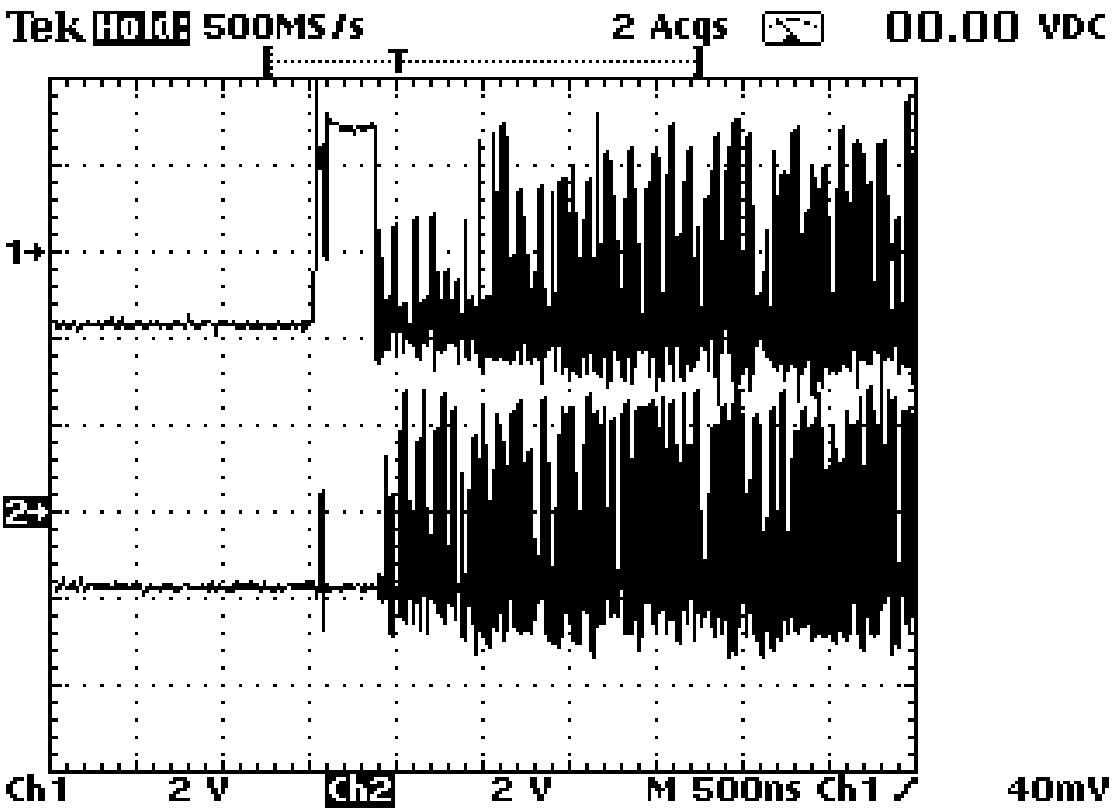
First experience: oscillations without any signal, both on the SEU and trigger lines.

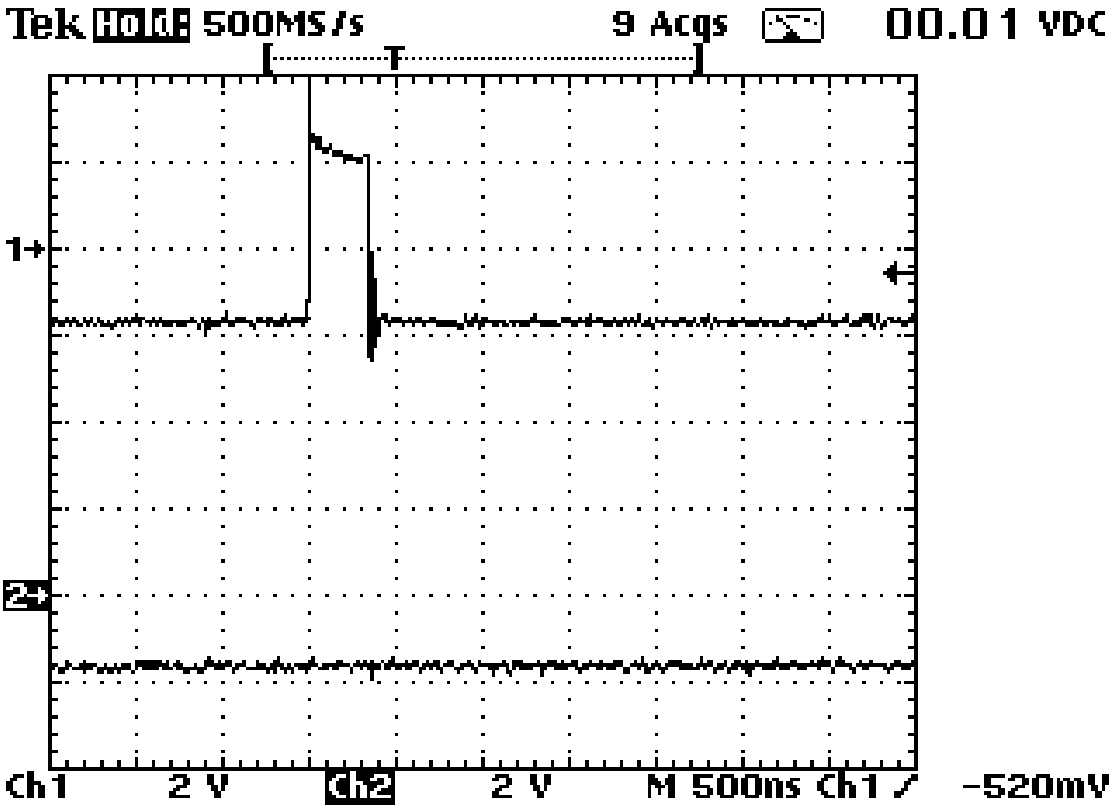
After some witchcraft we managed to get rid of the problem by separating the trigger lines from the rest (in the cable sections where the twisted pairs are loose).

Still: the response of the comparator is much faster than needed, any switching in the VADAQ (e.g. between monitoring of various quantities) is enough to produce signals, thus faking the *seub* occurrence.

$\rightarrow$ Samo is working on a circuitry which would hopefully filter this out,
$\rightarrow$ and tries to remove the witchcraft part from the elimination of ringing.


Tek HOLD 1GS/s
73 Acqs
00.00 VDC
1+
2+
Ch1 2 V Ch2 2 V M 20ns Ch1 ∕ 440mV


Tek HOLD 500MS/s
2 Acqs
00.00 VDC
1+
2+
Ch1 2 V
Ch2 2 V
M 500ns Ch1 ∕
40mV

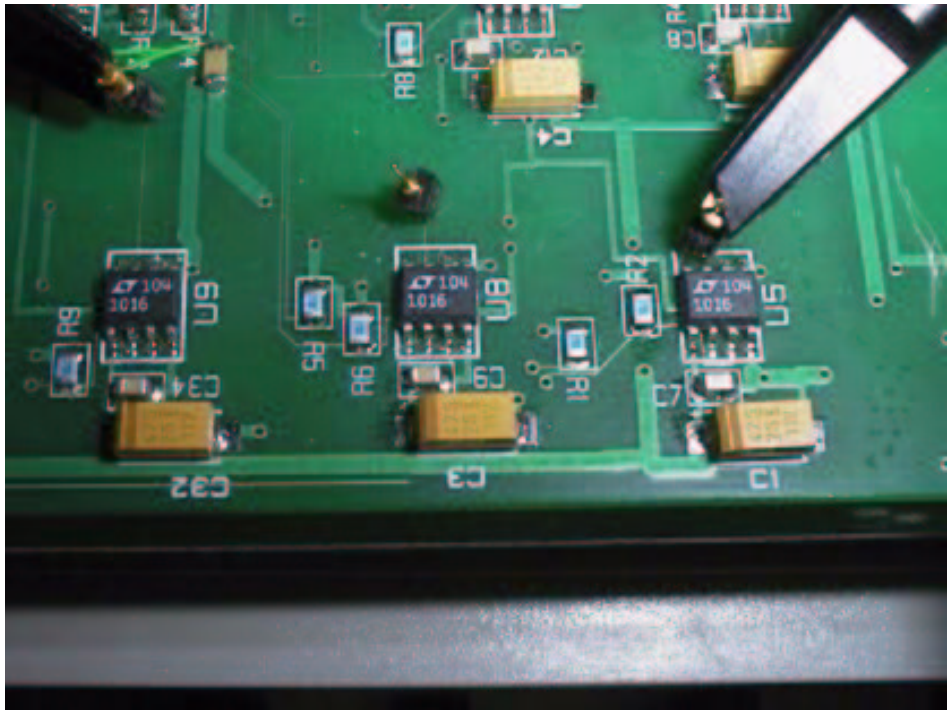

Tek HOLD 500MS/s
9 Acqs
00.01 VDC
1+
2+
Ch1 2 V
Ch2 2 V
M 500ns Ch1 ∕ -520mV

Present status as of yesterday:

A short with a capacitor of 20-100 pF on the *seub* comparator input improves the signal - no ringing also on the trigger inputs

Seems to be related to the fact that the cables are connected with 120 Ω to the ground, which makes differentially 240 Ω. Well matched?

→ Under study: pair termination of all lines



SEU correction

SEU protection: majority logic

Serial shift register structure

The serial shift register used for slow control is implemented with flip-flops specially designed to be SEU tolerant. A schetch showing the principle of these cells is shown in figure 8. Bits are shifted into the cell through the *D* pin into the D-flip-flop by applying pulses at the external clock pad. The output of the DFF is shifted out through the *Q* output pin. When all bits have been shifted to the correct place in the serial shift register, a pulse should be applied to the *load* pin. This will open the latches, and store the value of the DFF in the three parallel latches. The stored values in the latches are seen by two different blocks of sequential logic. The *Majority selection module* outputs the logic value that the majority of the latches store. This logic value is the value that is actually used by the chip logic, and is output through the *valid bit* pin.

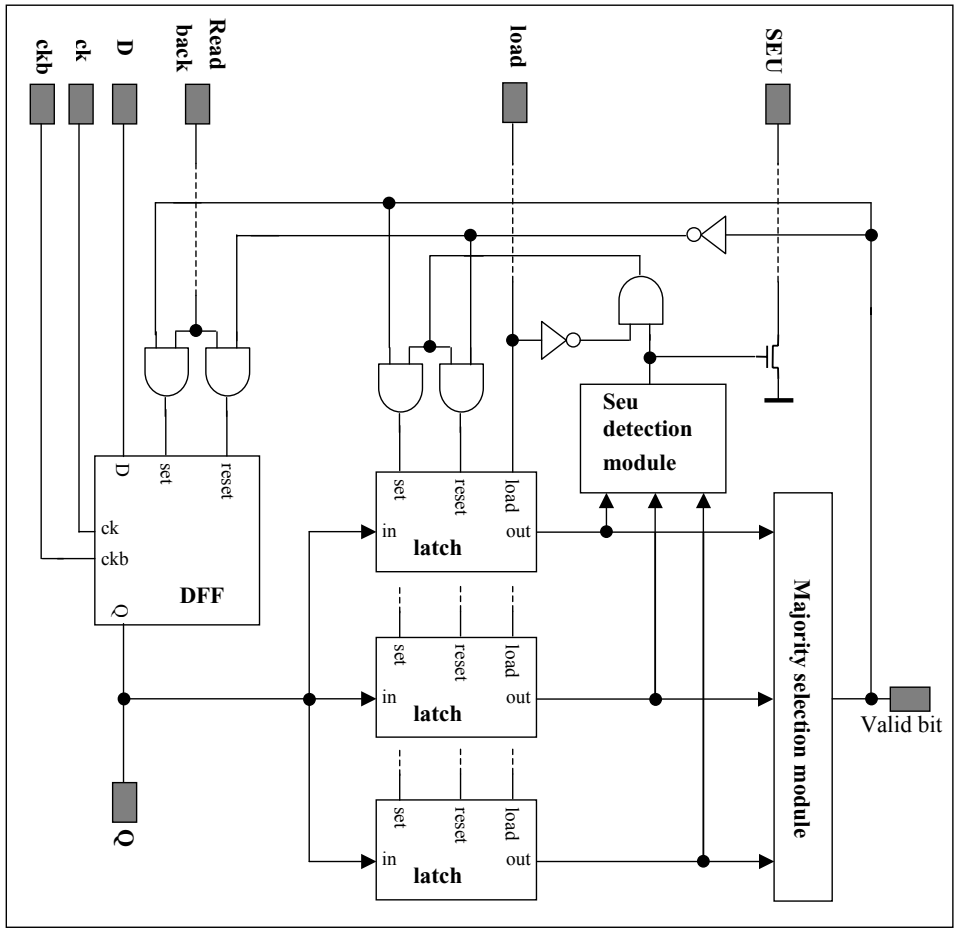


Fig. 8: Overview of the architecture of a SEU-flip-flop.

Control register

The Va1Ta chip contains a 680 bits long shift register which can be loaded serially using *RegIn* (serial data) and *ClkIn* (clock). A more thorough description of the contents of the register is found below and in figure 9.

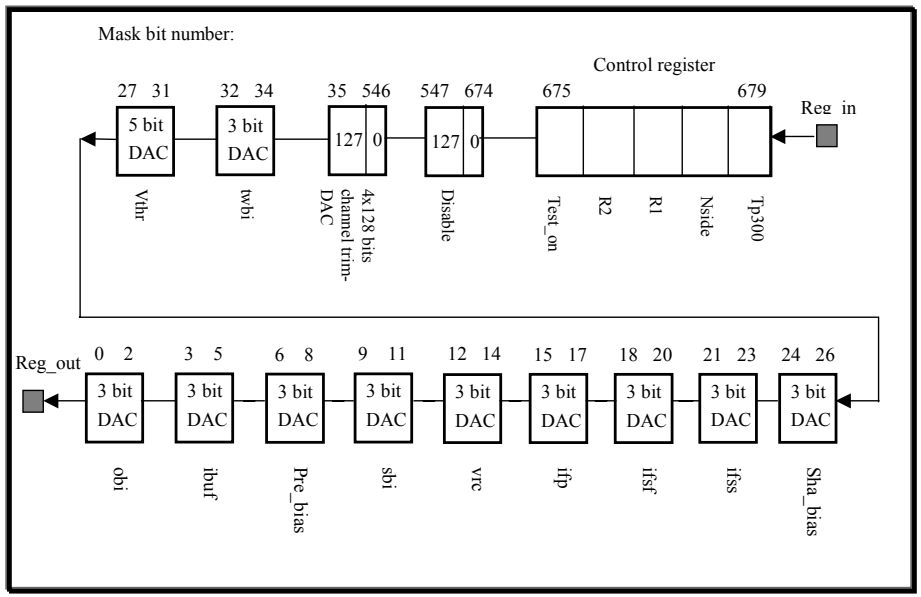


Figure 9: The sequence of the serial shift register mask. The sequence numbers are shown at the top of the boxes. Bit 0 is the first bit to be loaded. The channel numbers are indicated inside the boxes for the channel disable register and the channel threshold DAC register.

The serial shift register is shown in figure 9. The bits in the control register have the following function. A "1" in *Tp300* sets the peaking time of the fast shaper to 300ns. "0" sets the peaking time to be 75ns. A "1" in *nside* will prepare the channel for negative input signals. This control signal affects both bias generation and channel logic. The bits *R1* and *R2* controls the feedback resistor in the preamplifier, and are described in table 1. In test mode, the *test_on* –bit must be set (in addition to a bit in the *test enable* –register). The channel *disable* –register disables any channel with a high bit.

seub: where does it help?

- *seub* output only records (and corrects) a problem that occurred in the slow control register part
- no monitoring, no protection in the clocking through of the channel output enable shift register, *shift-out*, *shift-in*

SEU correction circuit: a possible way of use

- watch the *seub* output
- if *seub* fires, clock the currently stored slow control register values out (and simultaneuosly clock in the should be values)
- compare with should be values
- if different, act

Clocking out could be also done periodically as a kind of monitoring.

Summary, plans

- Looks like we can finally move back to the solid state lab and do the proper high power laser test by monitoring the bias and supply currents and watching the *seub* output.
- We will try to include *seub* monitoring in the VADAQ software.
- A slightly upgraded VADAQ library is already available on the web.
- We hope that our experience with running the hybrid will be also of use to other users.