A candidate for front-end read-out of the aerogel RICH

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Functional description

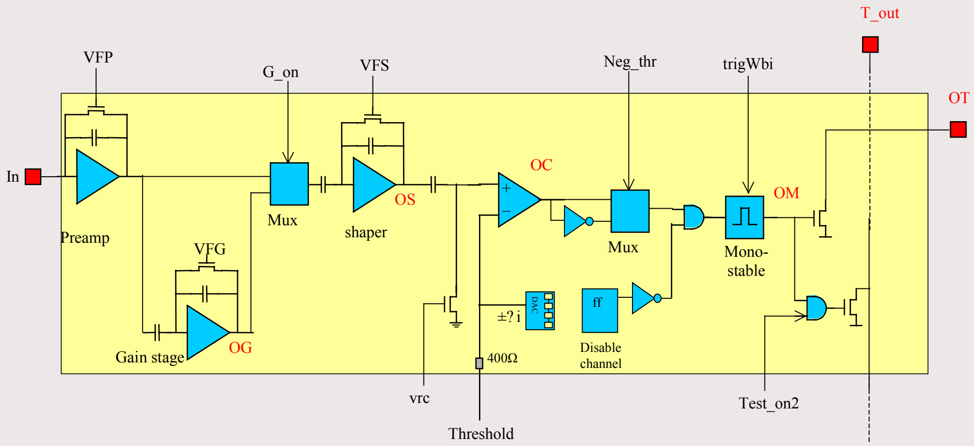

Fig 5. VA64Tap Channel Architecture

The Va64Tap channel is shown in the figure above. After the preamplifier, the signal path is split in two. Depending on the setting of the global control bit "*g_on*", the input of the shaper is connected to either the preamp or the gain stage. The gain stage has inverting gain, meaning that the polarity of the threshold and the value of the control bit "*neg_thr*" need to be changed. The noise filtering shaper has a peaking time of ~70ns. A high pass filter is situated after the shaper to remove offsets on the input signal to the discriminator. The Discriminator offset is also reduced by a 4 bit trim-DAC. The trim-DAC adds or subtracts current through a resistor placed in series with the global on-chip threshold line. The DAC has 1 mV steps with nominal biases. When tuning the DACs, optimal performance is obtained if the current from the trim-DACs in the various channels zeros out, meaning no net current is flowing out of the chip.

The discriminator output *OC* should be inverted by selecting the inverted output if the discriminator threshold is negative. This is done by setting the control bit "neg_thr".

Setting the according channel bit in the disable register can disable any channel. If the channel is not disabled, a signal that triggers the discriminator will be formed into a pulse with a duration controlled by the "*trigWbias*". The parallel trigger output *OT* is an open-drain current that should be terminated with a low impedance in order to avoid pick-up in other channels. It can be connected directly to the input of the LS64 ASIC.

An additional feature is implemented in the channel to facilitate testing. If the global control register bit *test_on2* is set, an additional trigger output *t_out* is enabled. The t_out is available

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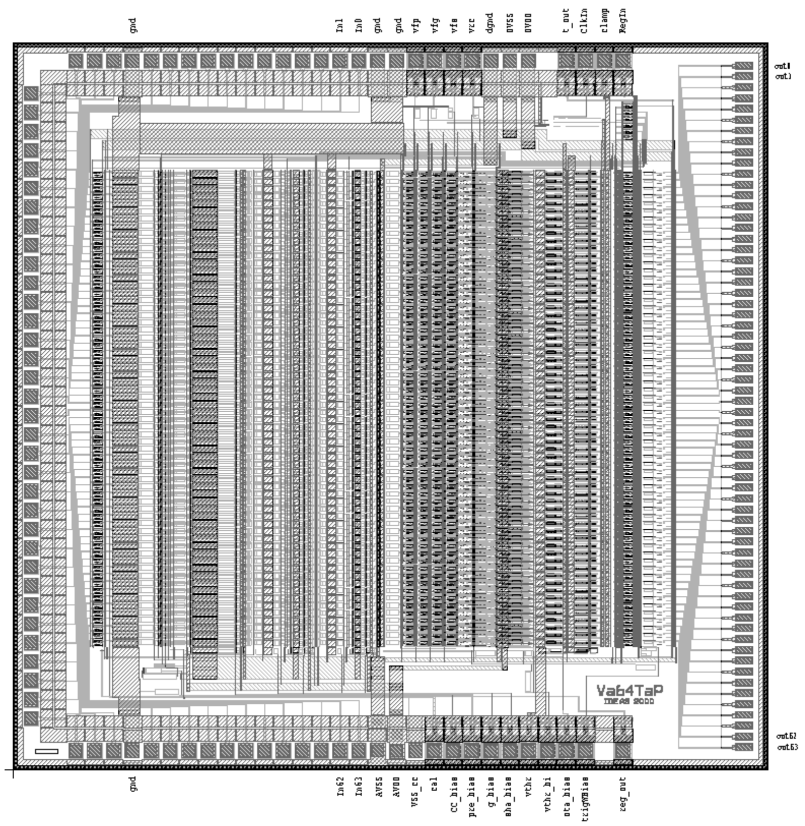
VA64TAP

Documentation v0.94



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General

The Va64Tap is a low-power, low noise ASIC optimised for moderate detector capacitances (~10pF). The preamplifier has high gain. There is a gain-stage after the preamplifier, which is possible to disable with a bit in the control register. The output of the gain stage/preamplifier is filtered by a CR-RC fast shaper with a peaking time of 75ns. Each channel has a discriminator, with a 4-bit trim-DAC to reduce threshold spread. The ASIC has 64 parallel trigger outputs, one for each channel. The trigger is encoded as a current, and should be terminated with low impedance.

Physical

• Process:	0.8 µm N-well CMOS, double-poly, double metal.	
• Die size:	5605 µm x 5380 µm	
	Thickness: ~ 600 µm	
• Input bonding pads:	Single row on three sides.	
	Pad size:	90 µm x 90 µm
	Pad pitch:	140µm (see. fig. 2)
• Output pads:	Single row on one side.	
	Pad size:	50 µm x 120 µm
	Pad pitch:	80 µm (see fig. 2)
• Control and power pads:	Single row on upper and lower side.	
	Pad size:	90 µm x 90 µm
	Pad pitch:	140 µm (see fig. 2)

Highlights of specs

- ENC: 500e- @ 10pF and 75ns Tp
- Threshold uniformity: ±200e-
- Threshold nominal value: 3000e-
- Fall time shaper: <10% @200ns

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LS64 is a pad limited chip. The chip has 64 data inputs and a similar number for data outputs. There are 4 input bias pads, 2 for current biases and 2 for voltage biases. The chip is supplied with 4 power supplies, each with a pad. The following table summarizes the pad structure beginning clockwise from top left:

Pad name	Type	Description	Nominal value
Ibias2	ai	Input current bias	200? A
Vbias2	ai	Input voltage bias (internally generated)	0.5 x (DVDD + DVSS)
DVSS	p	Digital VSS	0 V
DVDD	p	Digital VDD	2.5-5 V
AVSS	p	Analogue VSS	-2 V
AVDD	p	Analogue VDD	2 V
Vbias1	ai	Input voltage bias (internally connected to DVSS)	0.5 x (AVDD + AVSS))

5. Layout

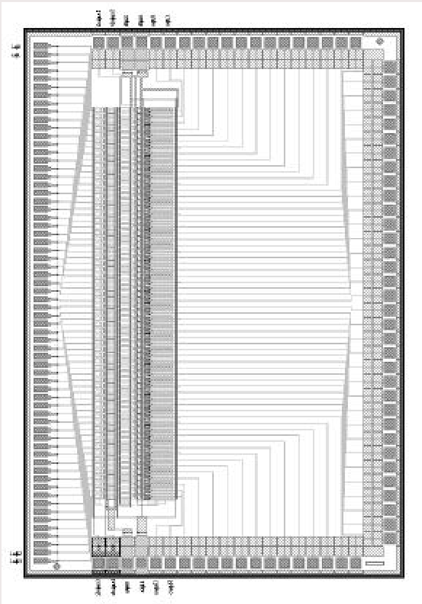

Fig. 1 Chip plot of LS64

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Status, plans

- Both chips are in our hands.
- Printed board is being designed to accept both chips.
- We have started to look into the question of how to drive them. Hopefully some upgrade of the VA1TA scheme.

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